III-V SEMICONDUCTOR PROCESSING: CONTACTS, ETCHING, AND DEVICES

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Abstract of Dissertation Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Doctor of Philosophy

III-V SEMICONDUCTOR PROCESSING: CONTACTS, ETCHING, AND DEVICES

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Chairman: Fan Ren
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Semiconductor processing of III-V materials is a vast topic, but this dissertation focuses on contacts, etching, and devices in very specific ways. The first chapter investigates the use of e-beam deposited SiO and SiO_2 to prevent galvanic effect etching of AuGe contacts for GaAs intergrated circuits. In the second chapter, the material characteristics of e-beam deposited SiO and SiO_2 as hydrogen free dielectrics are studied. The third chapter shows how the overhang visible on the (011) GaAs cross-section can be eliminated during wet-etching, making metallization possible in any direction. Chapter four discusses the fabrication of PNP InGaAsN heterojunction and double heterojunciton bipolar transistors for low power applications. Chapter five shows the first efforts of our group in the field of spintronics. Fabrication methods for processing a spin field effect

transistor on an InGaAs/InAlAs system are explored. Finally, chapter six outlines testing of spin field effect devices and the group's ongoing efforts in this area.

CHAPTER 1
THE USE OF AMORPHOUS SIO AND SiO_2 TO PASSIVATE AUGE BASED CONTACT FOR GAAS ICS

1.1 Introduction

Recently, GaAs based transistors have been widely used for the wireless applications owing to its high electron mobility, high saturation velocity, and availability of semi-insulating substrate.[1,2] During the device fabrication, the exposure of unpassivated GaAs to wet chemical etchants or atmospheric conditions leads to oxidation of the GaAs layer for several nanometers and this oxide layer will be removed prior to the deposition of the dielectric passivation layer.[3] However, after metallization, the GaAs etch rate greatly increases in close proximity to the metal contact regions during the oxide removal step and thus degrades device performance due to the increases of parasitic resistances. This is due to the Galvanic cell effect; the metallization has different electric potential from the semiconductors and will enhance the semiconductor etch around the metal contacts. Without the proper passivation, a trench around the metallization with few thousand Å depth can be obtained and devices will degrade significantly.[4] A thin Ti was used to cap AuGe based ohmic contact system to prevent the trench etch effect.[5] However, the thickness of Ti layer needs to be less than 100 Å to ensure the entire Ti layer is oxidized during the ohmic metallization alloyed to prevent the trench etch effect, and to prevent oxygen diffusion into the AuGe based metallization. Oxygen diffusion increases the contact resistance between the interconnect and ohmic metallization.

In this work, an E-beam deposited amorphous SiO or SiO_2 was used to passivate the metal contacts, both Schottky and ohmic metal, to avoid the trench etch effect. The effectiveness of the passivation will be assessed by analyzing data from the TLM measurements, and Auger analysis. The etching characteristics of SiO and SiO_2 in HF, BOE and CF_4/O_2 were also investigated.

1.2 Background

1.2.1 Bandgap

Each band corresponds to a different orbit (subshell), such as S, P, D, or F. In crystalline solids different directions have different band energies along their axis. The projection of one band direction upon another shows that the band energies overlap. This overlapping results in orbital hybridization. As a result some valence electrons expected to be in an S orbital will actually be in a P orbital. However, depending on the material, there may not be enough valence electrons to "fill" the band to establish a large density of states at the Fermi level.

In metals overlapping is so extensive that semi-continuous energy states are allowed, and the material is conductive. In insulators, the projection of one band direction upon another shows large forbidden energy regions (the bandgap) between orbitals. However, in semiconductors such bandgaps are often small, and carriers can be excited relatively easily across the gap.[6]

For intrinsic semiconductors at room temperature the fermi level is located in the middle of the bandgap. Some electrons have been excited across the bandgap leaving some electrons in the conduction band, and electron vacancies (holes) in the valence

band. To make semiconductor devices, impurities (called dopants) are placed in the semiconductor that provide extra electrons or holes due to unsatisfied bonds orbitals. If these dopants provide electrons they are called donors (or n-type dopants); if they provide holes they are called acceptors (or p-type dopants). These donors and acceptors move the fermi level in the bandgap in relation to their activation energy. For donors, activation energy corresponds to distance of the fermi level from the conduction band. For acceptors activation energy corresponds to fermi level distance from the valence band. Electrons are excited into the conduction band, while holes are excited into the valence band. These excited electrons or holes are known as carriers and conduct current. This is shown in figure 1-1.

For n-type or p-type semiconductors the carrier density is related to the doping and the activation energy. A low activation energy means that there will be more carriers at a given temperature and doping. At room temperature the carrier density for shallow donors and acceptors (dopants close to their respective bands) is usually assumed to be equal to the doping concentration.

1.2.2 Current Transport Processes

Depending on barrier height, temperature, and material qualities such as doping concentration, carrier transport across metal-semiconductor contacts takes place by several different mechanisms. These forms are represented in figure 1-2, and they are the following:

1) Transport of electrons from the semiconductor over the potential barrier into the metal.

2) Quantum mechanical tunneling of the electrons through the barrier.

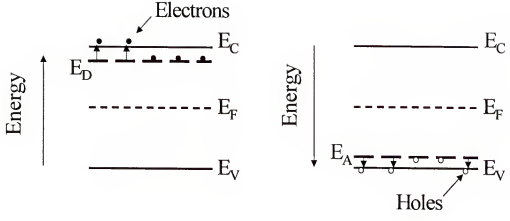


Figure 1-1: Band structure of donors (E_D) and acceptors (E_A). The band gap (E_g) is the distance between the conduction band (E_C) and the valence band (E_V) measured in electron volts (eV).

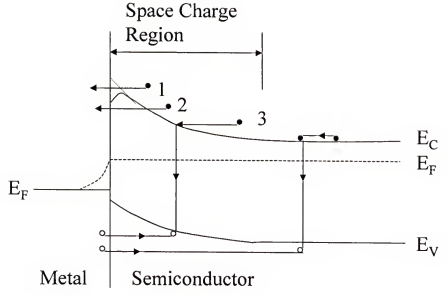


Figure 1-2: Four basic transport processes under forward bias.[7]

3) Recombination in the space charge region.

4) Hole injection from the metal to the semiconductor (equivalent to recombination in the neutral region).

The equations that describe current transport are based upon which of the four mechanisms dominate given assumptions made regarding current transport. The basic relations are laid out in the following paragraphs.[7]

Thermionic emission (mechanism 1) is derived from three assumptions:

1) The barrier height (ϕ_{Bn}) is much larger than the thermal energy (kT).

2) Thermal equilibrium is established at the plane that determines emission.

3) The existence of a net current flow does not affect equilibrium.

These assumptions mean that current flow through the contact is only dependent on the barrier height; barrier profile is not important. The equation for total current flow (J) that results is based on temperature (T), the applied voltage (V), electronic charge (q), the Boltzman constant (k), and the saturation current density (J_{ST}). This equation is the following:[7]

$$J = J_{ST}\left[\exp(\frac{qV}{kT}) - 1\right]$$

The saturation current density (J_{ST}) is dependent on the barrier height (ϕ_{Bn}) and Richardson's constant (A*):

$$J_{ST} = A^{*}T^{2}\exp\left(-\frac{q\phi_{B}}{kT}\right)$$

where the Richardson constant is equal to[7]

$$A^* = \frac{4\pi q m^* k^2}{h^3}$$

Here m* is the effective electron mass.

Diffusion theory is valid for lightly doped semiconductors where the width of the space charge layer is longer than the carrier diffusion length.[8] This theory is based on four assumptions. They are

1) The barrier height (ϕ_{Bn}) is much larger than the thermal energy (kT).

2) The effect of electron collisions within the depletion region is included.

3) Carrier concentrations in the space charge region are at equilibrium.

4) The doping of the semiconductor is nondegenerate.

The current still conducts by mechanism 1 (from figure 1-2), but the total current density (J) equation that results (neglecting image force lowering) is now

$$J = J_{SD}\left[\exp(\frac{qV}{KT}) - 1\right]$$

The saturation current density (J_{SD})for diffusion theory is

$$J_{SD} = \frac{q^2 D_n N_c}{kT}\left[\frac{q(V_{bi} - V)2N_D}{\epsilon_s}\right]\exp\left(-\frac{q\phi_B}{kT}\right)^2$$

Here, D_n is the diffusion constant, N_D is the donor doping density, ϵ_s is the semiconductor permittivity, V_{bi} is the built-in voltage, N_c is the effective density of states in the conduction band. Saturation current density J_{SD} is more sensitive to voltage, but less sensitive to temperature than J_{ST}.[7]

An intermediate theory applicable to intermediate doped semiconductors is the thermionic-diffusion theory.[7] It takes into account recombination near the metal semiconductor interface (mechanism 3 in figure 1-2), optical phonon scattering, and

quantum mechanical reflection at the metal-semiconductor interface.[8] This results in the following equation for total current density (J):[8]

$$J = \frac{qN_C v_R}{(1 + v_R / v_D)} \exp\left(-\frac{q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

where v_R is the recombination velocity, and v_D is the diffusion velocity of the electron.

Tunneling (mechanism 2 in Figure 1-2) may be the dominant mechanism for heavily doped semiconductors or operation at low temperatures.[7] The resulting equation is

$$J = J_S\left[\exp\left(\frac{qV}{nkT}\right) - 1\right]$$

but for V>> kT/q

$$J \cong J_S \exp\left(\frac{qV}{nkT}\right)$$

where J_S is found by extrapolating the log of the current density at V=0 from the linear region of the log-current vs. voltage curve. The ideality factor (n) in the above equation is defined as

$$n \cong \frac{q}{kT}\frac{dV}{d(\ln J)}$$

is an important factor in evaluating current flow.[7] At low dopings and high temperatures n~1 for metal-semiconductor contacts. However, if doping is increased, or the temperature lowered this ideality can increase substantially. It turns out this relation is also important for evaluating the quality of p-n heterojunctions (as will be seen in chapter 4). For heterojunction n~1 is an ideal junction, while n~2 indicates the dominance of

recombination current. Values between 1 and 2 represent varying degrees of recombination.

1.2.3 Contact and Sheet Resistance

In general there are two types of metal-semiconductor contacts, ohmic and schottky (or rectifying). Ohmic contacts have linear current vs. voltage curves, when an ohmic to semiconductor to ohmic contact system is biased. Schottky contacts only conduct when forward biased or when reverse breakdown occurs, when a schottky to semiconductor to ohmic contact system is biased. When a schottky to semiconductor to schottky system is biased (also known as back to back diodes), one contact is always reversed biased. This system only conducts when the reverse biased contact reaches breakdown. The generalized current vs. voltage curves for these contacts are shown in Figure 1-3.

Forward bias decreases band bending in the space charge region (shown in Figure 1-2). This decreases the barrier to current flow. Reverse bias increases band bending, increasing the barrier to current flow. A material can be reversed biased with very little current flow until tunneling electrons acquire enough energy so that their collisions with other electrons (in the space region) release electrons whose collisions release still more electrons and so on. This is known as reverse breakdown (or avalanche breakdown).[7]

Schottky contacts are used in field effect transistor applications as gate structures to modulate current flow. Ohmic contacts are critically important because current is conducted through them in the source and drain contacts of field effect transistors, and the emitter, base, and collector contacts of bipolar transistors. Therefore, high ohmic contact resistance means high series resistance, which leads to undesirable internal power

dissipation in a transistor. The series resistance includes the resistance of the metal itself, the contact resistance, the semiconductor region just below the contacts, and the resistance of the current passing through the semiconductor between the ohmic contacts (channel resistance). The channel resistance, also called the sheet resistance, is important because it contributes to the series resistance, and because it can be indicative of the material quality of the semiconductor when compared with known values.

Different methods have been generalized for ohmic contact and sheet resistance determination. The method that will be outlined in the following paragraphs is the transmission line method (TLM) proposed by Shockley.[9,10] In this method, identical ohmic contacts are deposited at varying distances from each other. The contacts are deposited on a mesa to minimize current spreading, which can spuriously increase resistance. Current is passed between adjacent contacts and the resistance is recorded. By plotting resistance vs. contact spacing and fitting a line to it, the sheet resistance (ρ_s) and the specific contact resistance (ρ_c) can be calculated. A typical TLM test structure and resistance vs distance plot is shown in figure 1-4.

The total resistance (R_T) from current passed between two contacts is given by

$$R_T = \frac{\rho_s d}{Z} + 2R_C$$

where d is the contact spacing, Z is the contact width, and R_C is the transfer resistance (usually reported in Ω-mm). The transfer resistance is given by

$$R_C = \frac{\sqrt{\rho_s \rho_c}}{Z} \coth\left(\frac{L}{L_T}\right)$$

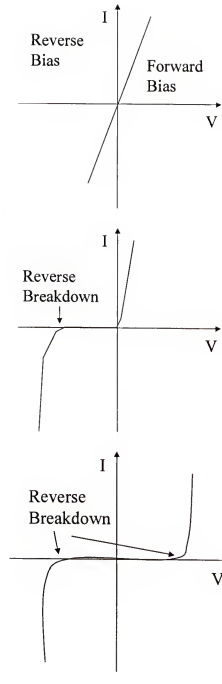


Figure 1-3: Metal and semiconductor contacts. Ohmic to semiconductor to ohmic contact system (Top). Schottky to semiconductor to ohmic contact system (Middle). Schottky to semiconductor to Schottky contact system (Bottom).

and can be determined from the y-intercept of the line fitted to the resistance vs. contact spacing (d) graph (see figure 4). Here L is the contact length, and L_T is the transfer length. The transfer length (L_T) is

$$L_T = \sqrt{\frac{\rho_c}{\rho_s}}$$

or can be determined from the x-intercept of the line fitted to the resistance vs. contact spacing (d) graph (see figure 1-4). The transfer length is the length (L_T) of the metal contact where the voltage drop of the current transferring from the metal contact to the semiconductor has dropped to 1/e of its maximum value.[10]

The sheet resistance (ρ_s) is usually reported in Ω/square and is determined from the slope (m) of the line fitted to the resistance vs. contact spacing (d) graph by

$$\rho_s = mZ$$

Using these equations the specific contact resistance (ρ_c) (usually reported in $\Omega\text{-cm}^2$) can be calculated. For $L<.5L_T$ specific contact resistance (ρ_c) can be simplified to

$$\rho_c = LZR_C$$

or for $L>1.5L_T$

$$\rho_C = L_T ZR_C$$

It should be noted that for this method the sheet resistance is assumed the same under and between the ohmic contacts. The TLM method is often done using four probes, two

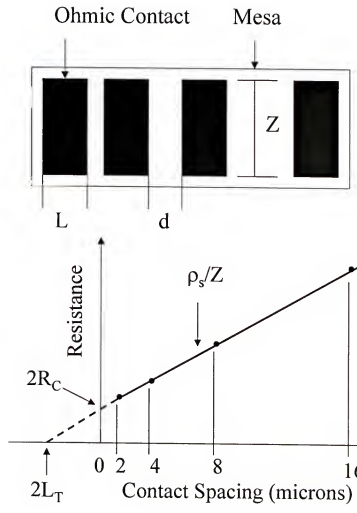


Figure 1-4: TLM testing. TLM test structure (top). Resistance vs. contact spacing of TLM measurement (bottom).

on each contact. Current is passed between two contacts, while the voltage drop is measured across the other two. This eliminates the probe resistance from being included in the total resistance (R_T).

1.3 Experimental

A metal organic chemical vapor deposition (MOCVD) grown Si-doped n^+/n (1000 Å, 3×10^{18} cm^{-3}/ 1200 Å, 2×10^{17} cm^{-3}) GaAs MESFET structure was used to fabricate the transmission line method (TLM) patterns. The TLM mesa was defined with wet chemical etch and the conventional AuGe based metallization was utilized for the ohmic contact. Samples passivated with a SiO_2 or SiO layer were prepared by depositing a 300 Å dielectric on the top of ohmic metallization without breaking the vacuum from SiO and SiO_2 sources, as shown in figure 1-5.

The samples were etched in DI water, and 20/1 H_2O:HCl. The GaAs native oxides and GaAs epi-layer etching were monitored with the TLM measurements. To study the etching characteristics of SiO and SiO_2 in wet chemical and dry etchings, a 3,000 Å of SiO and SiO_2 was deposited on GaAs substrates and AZ 1818 was used as the etch mask. For the wet chemical etching, etchings in BOE and 20/1 H_2O/HF were investigated. For dry etching, 96% CF_4 balanced with O_2, $5SF_6$/10Ar, and $5NF_3$/10Ar gas mixtures were utilized and Micro-RIE as well as Plasma Therm 770 inductively coupled plasma systems were used to etch to dielectrics. Auger analysis was performed on the un-annealed and annealed SiO or SiO_2/AuGe/GaAs samples to examine the interface between dielectric and ohmic metallization.

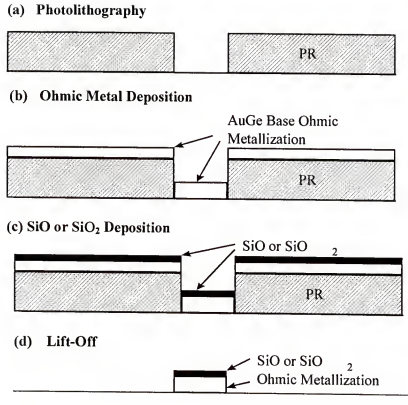


Figure 1-5: Schematic diagram of deposition ohmic metallization and passivation SiO_x layer.

1.4 Results and Discussion

As shown in figure 1-6, unpassivated samples have significant increases for sheet resistance even soaked in DI H_2O and degraded more severely in HCl solution. The resistance changes reach 20% when the soaking times in DI H_2O and 20:1 of H_2O:HCl solution are around 50 and 70 mins, respectively. However, samples passivated with a 300 Å evaporated either SiO or SiO_2, this Galvanic trench etching effect can be eliminated as illustrated in figure 1-7. There is virtually no changes of GaAs sheet resistance for both DI H_2O and 20:1 of H_2O:HCl solution soaking up to 40 min. The sharpness of silicon oxide/metal interfaces were examined with Auger depth profiling. As illustrated in figures 1-8 and 1-9, the Auger depth profiles of as deposit and annealed at 400°C for 20 seconds SiO/AuGe based ohmic metallization and SiO_2/AuGe based ohmic metallization samples, respectively, the oxide/metallization interfaces remained fairly sharp after ohmic metallization alloying for both SiO and SiO_2 passivation.

Unlike the Ti/AuGe based ohmic metallization system, there is no oxygen alloyed into the AuGe based metallization. The silicon oxides can be etched off with the conventional wet and dry etches through the contact via holes for the multi-level interconnection.

The wet chemical etching characteristics of SiO and SiO_2 were investigated and summarized in Table 1-1. The evaporated silicon oxides have slower etch rates than the PECVD SiO_2 and the etch rates of SiO are slower than that of SiO_2. From auger analysis, the evaporated SiO and SiO_2 are non-stoichiometric and oxygen deficient. The slower etch rates attribute to that oxygen deficient SiO_x has more Si-Si

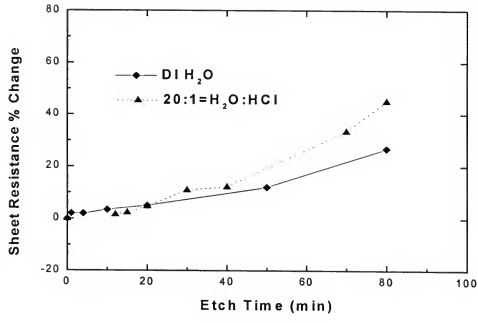


Figure 1-6: Sheet resistance % changes of unpassivation GaAs sample after DI H_2O and HCl solution soaking.

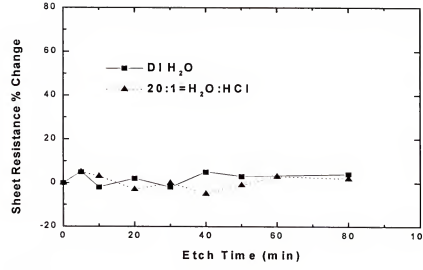


Figure 1-7: Sheet resistance % changes of SiO and SiO_2 passivated sample after DI H_2O and HCl solution soaking.

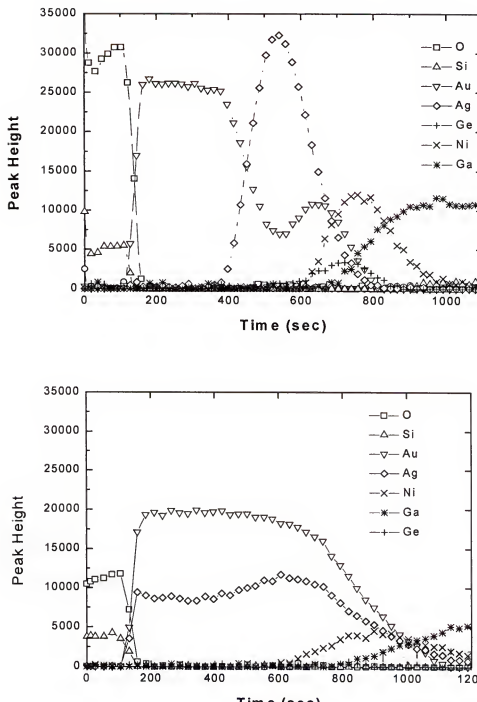


Figure 1-8: Auger depth profiles of SiO/AuGe based ohmic metallization/GaAs samples (top) as deposit (bottom) Annealed at 400 °C for 20 sec.

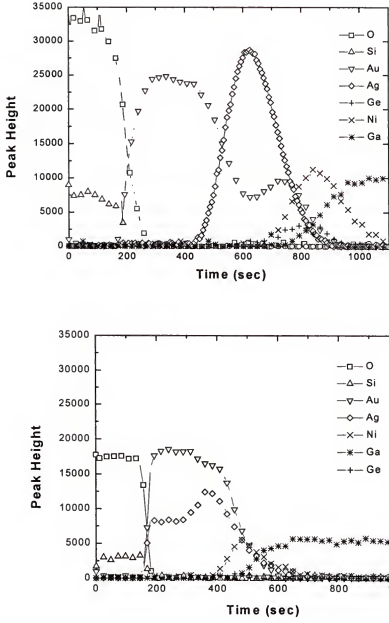


Figure 1-9: Auger depth profiles of SiO_2/AuGe based ohmic metallization/GaAs samples (top) as deposit (bottom) Annealed at 400 ℃ for 20 sec.

Table 1-1: Etch rates of SiO_2/SiO in dilute HF and BOE solutions.

Evaporated Oxide	**Solution**	Etch Rate (Å/min)
SiO	DI Water/HF (20/1)	109.8
SiO2	DI Water/HF (20/1)	162
SiO	BOE	50.36
SiO2	BOE	108

bonds than that of the stoichiometry SiO_2. It has been suggested that the polar Si-O bonds make the silicon backbone more vulnerable to charged acid/base elements. These elements induce polarity in Si-Si bond. The $Si\text{-}Si^+$ bonds are more susceptible to acid/base attack.[11] The dry etching of SiO and SiO_2 was also studied, as will be explained in chapter 2. A similar trend was obtained in dry etching. The SiO has slower etch rates in the SF_6 discharges.

1.5 Conclusions

The use of SiO and SiO_2 to passivate metallization and prevent the Galvanic etching effect was demonstrated. This technology can be used for GaAs IC fabrication to passivate the metallization during cleaning steps to avoid the trench etching effect. The passivating silicon oxide layer can be deposited on top of the metallization without breaking vacuum and the oxide layer can be etched off with the conventional wet chemical or dry etching.

CHAPTER 2
WET AND DRY ETCHING CHARACTERISTICS OF ELECTRON BEAM DEPOSITED SIO AND SiO_2

2.1 Introduction

It is well known that hydrogen can unintentionally contaminate Si or III-V crystalline semiconductors at almost any step in the growth or fabrication process (such as plasma chemical vapor deposition or wet chemical etching). For example, hydrogen can be present in the form of water vapor, OH species in oxides, in silicon nitride, and in photoresists. These hydrogen sources may be an intentional process component (as in C_2H_6-H_2-Ar plasmas), or may result from leaks or reactor out-gassing.[12] Hydrogen exposure leads to shallow acceptor and donor impurities passivation in Si and GaAs.[13] Naturally, this results in increased resistivity and lower device switching speeds. Furthermore, in silicon, hydrogen (in the absence of plasma or radiation damage) has also been shown to induce microcracks (platelets) in the near surface region, and to form deep levels. In compound semiconductors, platelet formation has been observed in GaAs after proton implantation and high temperature annealing.[14] Therefore, as thermal budget and device dimensions continue to decrease, the control of unintentional hydrogen incorporation in device processing will become increasingly more important to device reliability and operation.

In chapter 1, we studied the effectiveness of E-beam deposited SiO and SiO_2 in blocking the trench etch effect by passivating the metal contacts on TLM structures on GaAs.[15] Essentially, this work showed that the etch current generated by the edge of the TLM contact metal was negligible as compared to the exposed surface of the top of the TLM contact. Therefore, by passivating the upper surface of the metal contact, the etch trench effect could be greatly reduced. TLM measurements indicated that the trench etch effect was suppressed in SiO and SiO_2 passivated contacts for periods up to 80 minutes during wet etching in H_2O and 20/1; H_20/HCl. During the same period unpassivated samples changed substantially. Auger analysis confirmed that a sharp interface was maintained between the AuGe metal contacts and SiO and SiO_2 interfaces. Wet etch results showed that SiO_2 etched faster in both BOE and 20/1; H_2O/HCl solutions. It was suggested that the enhanced etch rate of SiO_2 over SiO was due to the presence more highly polar Si-O bonds in SiO_2 acting as insertion sites for acid/base attack. We concluded that SiO and SiO_2 were effective in blocking the trench etch effect on GaAs substrates.

In this chapter, an E-beam deposited hydrogen free amorphous SiO or SiO_2 was used to passivate GaAs substrates to assess the film characteristics of the SiO and SiO_2 and to study process compatibility. Specifically, the GaAs passivated substrates were used to study the dry etch rates of SiO and SiO_2, and the refractive index of the deposited layers. The passivation of the metal contacts was done to assess the film morphology and pattern transmission.

2.2 Experimental

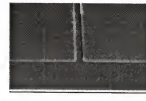
To study the dry etch characteristics of SiO and SiO_2, 3000 Å of SiO and SiO_2 was deposited on Si substrates and AZ 1818 was used as the etch mask. The dry etch gas mixtures were $5SF_6/10Ar$, and $5NF_3/10Ar$. These gas mixtures were used in Micro-RIE as well as Plasma Therm 770 inductively coupled plasma systems to etch the dielectrics.

Thermal stability of the films was studied with Auger, AFM, and ellipsometry. Auger was used to assess the Si/O ratio of the as-deposited films, and the films after they were annealed to 700 °C. AFM found the root mean square (rms) roughness of the as-deposited films and the 700 °C annealed films. Ellipsometry was then performed with an AutoEl IV on the SiO and SiO_2 samples to compare the refractive index of the as-deposited films and films annealed at 300, 500, and 700 °C for 20 seconds in an N_2 ambient.

2.3 Results and Discussion

Scanning electron microscope (SEM) photos reveal good morphology and edge definition before and after annealing for both SiO and SiO_2 (Fig. 2-1). The dry etching of SiO and SiO_2 was also studied, as illustrated in Figures 2-2 and 2-3. The SiO layer has slower etch rates in both SF_6 and NF_3 discharges under all conditions. Similar to our wet etch results (chapter 1), the slower etch rate of SiO_x has been attributed to more Si-Si bonds than that of SiO_2. It is believed that the polar Si-O bonds make the passivation layer more vulnerable to positive ion attack in the ICP plasma.[11,15] In figure 2-2

As-Deposited



SiO

SiO_2

Figure 2-1: SEMS of SiO/SiO_2 film deposition on TLM contacts.

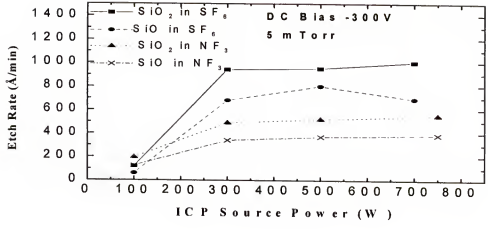


Figure 2-2: SiO/SiO_2 Film etch rate vs. DC bias in SF_6 and NF_3 discharges.

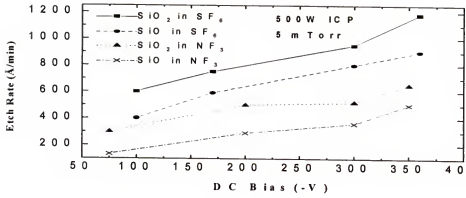
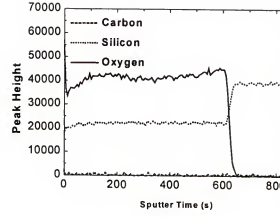


Figure 2-3: SiO/SiO_2 Film etch rate vs. ICP source power in SF_6 and NF_3 discharges.

increasing the D.C. bias causes a linear increase in etch rate due to a linear increase in energy of the ion bombardment. In figure 2-3 the etch rate of both SiO_2 and SiO saturate quickly with increasing ICP power. This is because the increasing ICP power quickly saturates the amount of ions generated in the plasma. SF_6 etched SiO_2 and SiO faster than NF_3 because it is able to generate more F atoms.

Auger analysis of the layers indicates that upon annealing to 700°C the Si/O ratio of SiO increases in the film (figure 2-4), while the surface Si/O ratio decreases from .62 to .54. This is consistent with oxygen flux to the surface during annealing. Figure 2-5 shows that the film Si/O ratio of SiO_2 remains constant both before and after annealing to 700°C. The surface SiO/O ratio remained constant as well. AFM of SiO (figure 2-6) reveals that the root mean square (rms) surface roughness decreases upon annealing to 700 °C from .364 nm to .263nm. This decrease in surface roughness may be related to the oxygen flux to the surface indicated in the Auger analysis. However, for SiO_2 film (figure 2-7), the rms roughness increases from .876 nm to 1.01 nm.

Ellipsometry was performed to assess the change in refractive index and thickness at different positions on the wafer, and the refractive index upon annealing. The refractive index of the as-deposited SiO varies considerably across the wafer (+/- .025), while the SiO_2 remains more constant (+/- .001). It has been shown previously, that e-beam deposition of SiO always results in Si/O≈1 regardless of deposition pressure and rate[16]. Therefore, spatial variance in refractive index may be more structural (such as surface roughness) than chemical. Both samples showed excellent thickness uniformity across the wafer varying at ≤ 2%. Figure 2-8 shows the refractive indexes of the annealed samples. The magnitude of the changes is relatively the same, and minor



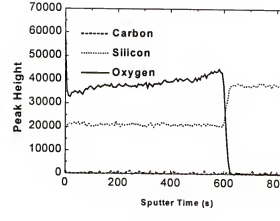
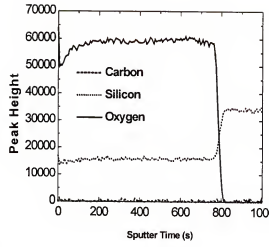


Figure 2-4: Auger depth profiles of 3000 Å SiO on Si as-deposit (top) and after annealing 700°C (bottom).



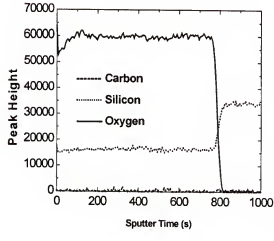


Figure 2-5: Auger depth profiles of 3000 Å SiO_2 on Si as-deposit (top) and after annealing 700°C (bottom).

Figure 2-6: 5 μm AFM of 3000 Å SiO on Si as-deposit (top) and after annealing 700°C (bottom). The vertical scale is 25nm.

Figure 2-7: 5 µm AFM of 3000 Å SiO_2 on Si as-deposit (top) and after annealing 700°C (bottom). The vertical scale is 25nm.

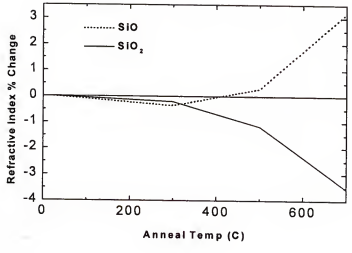


Figure 2-8: Refractive index change vs. anneal temperature for SiO/SiO_2 films.

(approximately +/-3% at 700 °C). However, the refractive index of SiO increases, while that of SiO_2 decreases over the temperature range. The increase in SiO refractive index has been linked to the increase in Si/O ratio upon annealing that is evident in Auger analysis of the layers on silicon. The decrease in SiO_2 refractive index was attributed to the increase in surface roughness of the film upon annealing.

2.4 Conclusions

The characteristics of hydrogen free SiO and SiO_2 passivation layers used to passivate metallization and prevent the Galvanic etching effect were studied. Both passivation layers showed good morphology and edge definition on metal contacts upon annealing. E-beam deposited SiO_2 and SiO had dry etch rates comparable to PECVD SiO_2. They also had similar magnitudes of refractive index change upon annealing. The SiO showed more spatial variation in refractive index between samples and less thermal stability than SiO_2. However, SiO was smoother before and after annealing. Therefore, we conclude that the use of E-beam SiO_2 and SiO is compatible with current processing technologies, but that the superior dielectric would be application dependent in view of the mixed thermal stability and roughness results.

CHAPTER 3
NON-CRYSTALLOGRAPHIC WET ETCHING OF GALLIUM ARSENIDE

3.1 Introduction

Some semiconductor devices have large feature sizes, the need for etch isolation, and require continuous metallization to both the top and the bottom of the etched features including some vertical cavity lasers and photovoltaic devices. Such profiles are routinely available from reactive ion etching and related dry etches. However, wet etching compound semiconductors, such as (001) GaAs, can give different profiles depending on the orientation of the mask with respect to the crystal. In some of these orientations a break in metal coverage can occur due to surface overhang of the GaAs. Since, wet etching of GaAs continues to be attractive in some cases due to the cost of dry etch equipment, and in some applications sensitivity to plasma damage, a non-crystallographic wet etch is desirable.

Common acid-based etches using sulfuric acid, hydrochloric acid, or phosphoric acid mixtures with hydrogen peroxide exhibit crystallographic etching, where the (011) cross section shows a different profile than the $(01\bar{1})$ section.[17] Isotropic etching of GaAs has been observed for high ratios of HCl to hydrogen peroxide performed at room temperature and at elevated temperatures.[17] These isotropic etches are unstable as they evolve Cl_2 gas and continually reduce in etch rate as the HCl is depleted. Figure 3-1 schematically illustrates typical profiles that are commonly observed in wet etching of GaAs.

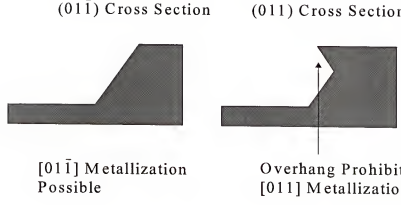


Figure 3-1: Cross sections of typical GaAs wet-etch profiles.

In this work, non-crystallographic wet etching of GaAs has been achieved by varying the masking material for acidic etches using phosphoric acid and hydrogen peroxide. Both a soft photoresist mask and a SiO_2 hard mask, that undergoes lateral erosion during the etch, have been used to create continually sloped profiles in both (011) and $(01\bar{1})$ sections. The conditions to create non-crystallographic etching have been analyzed.

3.2 Background

Gallium arsenide (GaAs) is a compound semiconductor arranged in a zincblende crystal structure shown in figure 3-2. In a zincblende structure, each atom is surrounded by four equidistant atoms that lie at the corners of a tetrahedron. For common reference, crystal planes are usually defined using Miller indices.[7] Miller indices are defined by finding the intercepts of the plane in terms of the lattice constant (a), and then by taking the reciprocals of these numbers and reducing them to the smallest integers having the same ratio.[7] The indices describing the planes found by this method are placed in an (hkl) format that corresponds to the (xyz) axis.[7] The graphical representation of this convention is shown in figure 3-2.

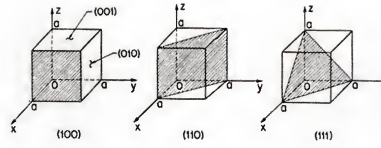
By extending this convention more aspects of crystal structure can be defined. A plane that intercepts x axis on the negative side is

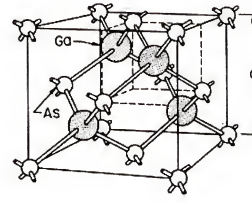
$$(\bar{h}kl)$$

where the bar over the h denotes the negative side of the x axis. Planes of equivalent symmetry are given by

$$\{hkl\}$$

where examples for {100} are (100), (010), (001), $(00\bar{1})$, $(0\bar{1}0)$, and $(\bar{1}00)$. Direction





ZINCBLENDE
(GaAs, GaP, etc)

Figure 3-2: Crystal planes defined by miller indices (Top) and GaAs zincblende crystal structure (Bottom).[7]

in a crystal is

$$[hkl]$$

such as [100] for the x axis. Finally a full set of equivalent directions is

$$\langle hkl \rangle$$

The ability to define crystal planes is important because different crystal planes in GaAs have different wet chemical etch rates; depending on the etch solution.[17,18] These etch rate differences cause anisotropy that may cause difficulty in semiconductor metallization schemes. Another important crystal structure property, cleavage planes, allows us to analyze how GaAs crystal planes are etched. For GaAs the cleavage planes are along the {110} planes.[7] By fracturing GaAs along the appropriate plane, we can observe (using a scanning electron microscope) how an etch progresses. Typical etch cross sections are shown in figure 3-1. It is seen that the (011) cross section is problematic for metallization.

Typical etch solutions for GaAs are acid/base/water solutions.[17,18] The water acts as a solvent, while the base oxidizes the GaAs, then the acid dissolves the oxide. In this work, the samples are etched with 1:4:45 H_3PO_4:H_2O_2:H_2O to etch the GaAs. Varying concentrations of 49% HF are added to 1:4:45 H_3PO_4:H_2O_2:H_2O to etch the SiO_2 hard mask.

3.3 Experimental

GaAs wafers were prepared by oxide removal with 20:1 H_2O/29.5 % NH_3OH for 30 seconds, followed by a dehydration bake at 120°C for 3 minutes. For soft mask preparation AZ4330 was spun onto the GaAs wafer at 4,000 rpm for 30 seconds to provide 3.5 μm of coverage. The resist was then baked at 90°C for 90 seconds. It was exposed for 6.5 seconds in a Karl Suss MJB3 aligner, and then developed for 150 seconds in 1:5 AZ 400K.

For hard mask preparation (after 20:1 H_2O/NH_3OH oxide removal and dehydration), ≅1,000 Å of SiO_2 was deposited by a Plasma Therm 790 PECVD reactor. The two GaAs wafers deposited with SiO_2 had refractive indexes of 1.478 and 1.456, and thicknesses of 1007 Å and 1053 Å (as measured by an AutoEl III ellipsometer at 6328nm). Then, the wafers were baked at 110°C for 20 minutes at 20 mtorr followed by 2 minutes exposure hexamethyldisilazane (HMDS) vapor at 110°C and 1-2 torr. This was accomplished in a Yield Engineering Systems (YES) model-585M Triple Function Bake-Vapor/Image Reversal/Silylation System. The HMDS enhances photoresist adhesion to the SiO_2. Three different photoresists were then spun onto cleaved wafer sections. AZ5214, AZ4330, and AZ4620 for resist thicknesses of 1.5, 3.5, and 6.4 μms respectively.

The AZ5214 was spun at 5,000 rpm for 30 seconds. It was baked at 90°C for 90 seconds. Exposure time 3 seconds in a Karl Suss MJB3 aligner. The pattern was then developed for 60 seconds in 1:5 AZ 400k. The AZ4330 was processed the same as it was for the soft mask. The AZ4620 was spun at 5,000 rpm for 30 seconds. It was baked at

110°C for 90 seconds. The pattern was exposed for 9 seconds, and developed in 1:4 AZ 400k for 150 seconds.

Both hard and soft mask samples were descummed after pattern development in an LFE PDS/PDE 301 barrel etch at 850 mtorr, 5 watts, for 4 min. After descumming, the photoresists were reflowed at 120°C for 3 minutes. To make this process more directly applicable to device fabrication, a HBT emitter mesa mask was used during etch experiments to more closely simulate solution loading and resist adhesion. The GaAs sample size was $1cm^2$. Prior to etching soft mask samples were immersed in 7:1 buffered oxide etch (BOE) to remove the SiO_2 not covered by the resist. Photoresist undercut was $\cong$.4 μm.

Soft mask samples (no SiO_2 between the photoresist and GaAs) were etched with 1:4:45 85% H_3PO_4/30% H_2O_2/H_2O (phosphoric-peroxide (PP) etch). Upon mixing, the 1:4:45 PP etchant showed a 2-3°C increase in temperature. An hour was sufficient for 1 liter to cool to 20°C for etching. The [100] etch rate in 1:4:45 was 50 Å/sec. Hard mask samples were etched with 1:4:45 H_3PO_4:H_2O_2:H_2O to etch the GaAs, as well as 1-5 ml of 49% HF to etch the SiO_2. The addition of HF to 1:4:45 increased the GaAs [100] etch rate slightly; at 6 ml HF to 100 1:4:45 the [100] etch rate was 63 Å/sec. To avoid etch solution depletion 100ml of 1:4:45 and 1-5 ml of HF were changed every 200 seconds ($\cong$1 μm) during etching. Furthermore, new solution was prepared every two days. Solution agitation changed direction every 100 seconds during etching. The resulting etch profiles were observed with a Jeol JSM 5,800 scanning electron microscope.

3.4 Results and Discussion

The hard mask samples with photoresist on top of SiO_2 show the overhang in the (011) plane cross section as seen in figure 3-3. They were etched with 1:4:45 H_3PO_4:H_2O_2:H_2O and the overhang in that crystal plane is typical of hard masks. On the other hand, the same phosphoric acid-based etch gave yielded (011) profiles without an overhang to depths up to 10 μm, as shown in figure 3-4 for a soft mask; which was AZ4330 photoresist. In figure 3-5 (etched in the same manner as figure 3-4), it is seen that the $(01\bar{1})$ plane has also etched without an overhang. Therefore, metallization is possible in any direction.

It should be noted that although smooth, sloped profiles were observed in both the (011) and $(01\bar{1})$ planes, the etches were not identical. The (011) cross section of figure 3-4 shows a slight rounding at the bottom of the profile under the mask edge that may indicate that the etch conditions are transitioning to a diffusion controlled etch. The profile of the $(01\bar{1})$ cross section of figure 3-5 is more indicative of a reaction rate limited that exposes a $(11\bar{1})$ plane. The 10 μm deep etches without overhang were achieved only if they were minimally agitated. With significant agitation, the photoresist loses adhesion to GaAs at shallower depths.

It is thought that the increased surface area caused by the (100) exposure (during lateral etch erosion) prohibits the formation of the overhang visible in the (011) cross section. Therefore, the etch rate can be somewhat decoupled from the shape of the crystallographic planes. This concept may in turn allow a greater tailoring of the crystallographic etch profile and etch rates when combined with etch solutions to

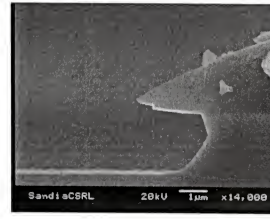


Figure 3-3: Cross Section of (011) plane etched 2 μm with 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is 1,000 Å SiO_2 and the resist is AZ4330.

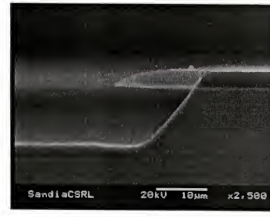


Figure 3-4: Cross Section of (011) plane etched 10 µm in 1:4:45 of H_3PO_4:H_2O_2:H_2O in the presence of AZ4330 soft mask.

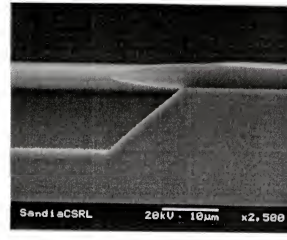


Figure 3-5: Cross Section of $(01\bar{1})$ plane etched 10 µm with 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is 1,000 Å SiO_2 and the resist is AZ4330

provide a wide variety of shapes.[17,18] This particularly seems true of the hard mask applications since the etch rate of the hard mask can be readily varied.

Dry etch processes yield reproducible sloped profiles in some processes because the photoresist mask erodes laterally in a slow but consistent way as the etch proceeds. An attempt to design a similar process to eliminate the overhang in the $(01\bar{1})$ plane using a wet etch is discussed next. A hard mask of SiO_2 with photoresist over it was evaluated with the addition of an etch component that erodes the mask as the GaAs is etched. These hard mask samples were etched with 1-5 ml of HF acid added to 100 ml of 1:4:45 PP etch. The addition of this quantity of HF changed the [100] GaAs etch rate by 20% or less, but made a big difference in the cross-sectional profile due to its effect in tailoring the mask profile. Hydroflouric acid at 2-4 ml provided sloped profiles suitable for metallization in AZ4330 and AZ4620 samples for depths up to 3 μm with or without agitation. After 3 μm, however, agitation becomes much more critical. High agitation degrades mask adhesion.

Good profiles also occur for deeper etches as long as agitation is minimal. When agitation near the threshold of vortex formation was used, the hard mask loses adhesion after 3 μm etch depth and profiles such as that in figure 3-6 occur for the addition of 3-4 ml of HF. At 5 ml of HF and above, the etch rate of the SiO_2 is faster than the lateral etch rate of GaAs, so that effective loss of the mask occurs and the etch profile also looks similar to that of figure 3-6. By minimizing agitation and reducing HF content to 2 ml, the suitable profile for the (011) plane was extended to 5 μm as shown in figure 3-7. The $(01\bar{1})$ cross section was similar in shape (though shallower in depth) to that of figure 3-5. At 5 μm, the etch profiles of the (011) and $(01\bar{1})$ planes are similar, and metallization is

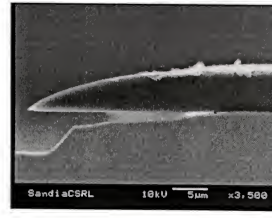


Figure 3-6: Cross Section of (011) plane etched 5 µm in 3 ml HF/100 ml 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is 1,000 Å SiO and the resist is AZ4330.

Figure 3-7: Cross Section of (011) plane etched 5 µm in 2 ml HF/100 ml 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is 1,000 Å SiO_2 and the resist is AZ4330.

possible in any direction. For etch depths greater than 5 μm, however, SiO_2 degradation increased considerably producing profiles such as figure 3-8.

At the lower HF concentrations of 1 and 1.5 ml to 100 ml 1:4:45 PP etch depths of 10 μms were obtained. However, the (011) etch profiles were not suitable for metallization, as can be seen in figure 3-9 and figure 3-10 respectively. Also, the (011) and $(01\bar{1})$ cross sections were no longer similar, since the $(01\bar{1})$ profile still resembled that of figure 3-5. These results show that HF concentration not only has an effect on limiting etch depth (with the proper profile) of the GaAs, but also that the GaAs etch profile can be greatly varied by altering the hard mask etch rate. Besides agitation and HF concentration, it was thought the photoresist itself limited the etch depth attainable for the hard mask samples. It was assumed that as the etch progressed, the photoresist would want to lift or peel back on itself, thereby imposing stress on the SiO_2. Since the tendency to lift was assumed greater in a thinner photoresist, AZ5214 was used to provide 1.5 μm. The results clearly show that the photoresist imposes such stress as seen in figure 3-11. In figure 3-12 it can seen that the stress induced failure results at the SiO_2/GaAs interface, no doubt accelerated by the HF present in the solution.

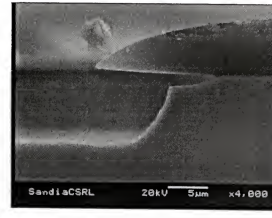


Figure 3-8: Cross Section of (011) plane etched >5 µm in 2 ml HF/100 ml 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is 1,000 Å SiO_2 and the resist is AZ4620.

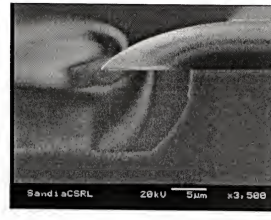


Figure 3-9: Cross Section of (011) plane etched 10 μm in 1 ml HF/100 ml 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is 1,000 Å SiO_2 and the resist is AZ4620.

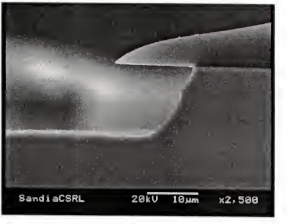


Figure 3-10: Cross Section of (011) plane etched 10 µm in 1.5 ml HF/100 ml 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is1,000 Å SiO_2 and the resist is AZ4620.

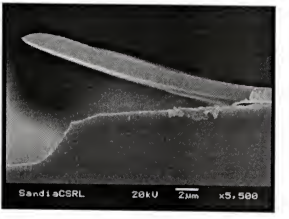


Figure 3-11: Cross Section of (011) plane etched 5 μm in 2 ml HF/100 ml 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is 1,000 Å SiO_2 and the resist is AZ5214.

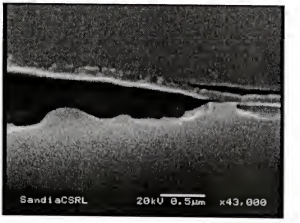


Figure 3-12: Stress/HF induced adhesion loss at the GaAs/SiO_2 interface after etching 5 µm in 2 ml HF/100 ml 1:4:45 of H_3PO_4:H_2O_2:H_2O. The mask is 1,000 Å SiO_2 and the resist is AZ5214.

3.5 Conclusions

Both soft and hard masks have been used to provide metallization suitable [011] wet etched profiles. It has been shown that for the AZ4330 soft mask that minimizing agitation in 1:4:45 H_3PO_4:H_2O_2:H_2O is essential to achieve etch depths of 10 μm. For the hard SiO_2 mask both agitation and HF concentration have to be minimized for etch depths. Photoresist thickness, however, should be relatively large to minimize the stress imposed on the SiO_2 by the photoresist. To increase the hard mask etch depth past 5 μm, perhaps the photoresist should be replaced with another hard mask or the hard mask itself should be replaced. These factors should be optimized to minimize stress on the hard mask, and to improve the hard mask/GaAs interface in a given etching solution. These results clearly show that mask interactions are as important to the etch profile as the etch solution. These concepts, combined with various etch solutions, should allow for greater tailoring of etch profiles at reasonable etch rates.

CHAPTER 4
INGAASN HETEROJUNCTION BIPOLAR TRANSISTOR

4.1 Introduction

In 1993 Sakai proposed that the addition of a small fraction of nitrogen into group III phosphides and arsenides results in a material with a smaller band gap.[21] This is believed to be due to the large band gap bowing caused by the large electronegativity of nitrogen.[21] Of these, InGaAsN has attracted interest because of its potential as a high temperature long wavelength laser for fiber-optic communications.[22,23] InGaAsN latticed matched to GaAs allows emission wavelengths longer than 1.2 μm, and at characteristic temperatures >150 K.[24] This is a great improvement over conventional InGaAsP/InP laser diodes whose characterisitic temperature is around 60k.[24] The higher characteristic temperature of InGaAsN is due better electron confinement due to larger conduction band offset.[24] Other uses of InGaAsN are for high-efficiency solar cells for satellites, and 1.45 μm light emitting diodes (LEDs).[23,25] In general, the development of low power InGaAsN is attractive because it is compatible with GaAs foundry technology; unlike expensive InP based technology.[26]

This chapter, however, will explore the use of InGaAsN in novel $Al_{.3}Ga_{.7}As/In_{.03}Ga_{.97}As_{.99}N_{.01}$ heterojunction bipolar transistors (HBTs), and $Al_{.3}Ga_{.7}As/In_{.03}Ga_{.97}As_{.99}N_{.01}/GaAs$ double heterojunction bipolar transistors (DHBTs). The use of $In_xGa_{1-x}As_{1-y}N_y$ as a base layer reduces power dissipation, because increasing

nitrogen concentration decreases the bandgap (E_g) to below 1.42 ev for GaAs. For the $In_{.03}Ga_{.97}As_{.99}N_{.01}$ used in this study the bandgap is decreased to ~1.2 eV. This smaller bandgap leads to a lower turn on voltage (V_{on}) for the device.[27] Also, it will be shown that nitrogen and indium incorporation can be used to manipulate conduction and valence band offsets to increase gain (by better carrier confinement).

4.2 Background

The bipolar transistor is a three terminal device with three ohmic contacts. They are located on the emitter, base, and collector layer. This device is a bipolar transistor because both electrons and holes contribute to the current flow. A small p or n-type current from the base to the collector should cause a much larger n or p-type (respective to whether the base is p or n-type) current to flow from the emitter to the collector. As such, the devices are known as p-n-p or n-p-n devices depending on the type of doping in the corresponding emitter-base-collector layers. Smaller band-gap highly doped regions are often added to the emitter and collector regions because they are easier to form ohmic contacts to. They are typically referred to as the cap layer and subcollector layers. A top view, and cross section of a typical circular emitter bipolar transistor is shown below in figure 4-1.

During transistor operation the base/collector junction is forward biased to inject holes into the base, while the base/collector junction is reversed biased to sweep the injected carriers into the collector. When the collector of this device is grounded, the gain (β) of this device is

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

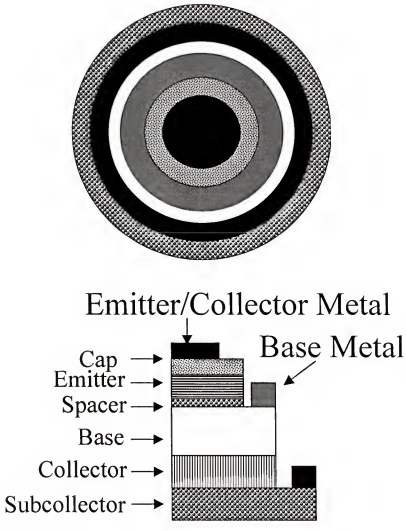


Figure 4-1: Top view (above) and cross section (below) of typical circular bipolar transistor.

where I_C is the collector current, and I_B is the base current. This is determined (most often) by sweeping the base and collector at the same voltage and by plotting the ratio of their currents to obtain β. This plot is called the gummel plot, an example of which is shown in figure 4-8.

Heterojunction bipolar transistors increase gain by using a wider band-gap material for the emitter. The band discontinuity created creates a barrier for carriers injected from the base contact to enter the emitter, reducing base current, thereby increasing gain.

Double heterojunction transistors also use a wider band-gap material at the base in order to increase emitter/collector breakdown voltage (BV_{ECO}). Emitter collector breakdown means that the emitter is shorted to the collector. In this case the device no longer functions as an amplifier.

4.3 Experimental

As nitrogen is incorporated into GaAs, a tensile strain develops (E_G is reduced). The addition of indium results in a compressive strain (reducing E_G). These strains are shown in figure 4-2. By balancing these two strains, $In_xGa_{1-x}As_{1-y}N_y$ can be latticed matched to GaAs when x equals approximately 3y.[23] Specifically, except for very low nitrogen, the addition of nitrogen to GaAs lowers the conduction band (E_C) and the valence band (E_v). [26] Indium also lowers E_C, but raises E_v. For the $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ emitter/base junctions (of both HBT and DHBT structures) the conduction band discontinuity (ΔE_C) is >.5 eV. The valence band discontinuity (ΔE_V) is only .15 eV. For the DHBT structure, the valence band discontinuity (ΔE_V) for the

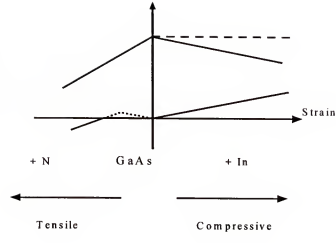


Figure 4-2: Qualitative effect of indium and nitrogen on conduction and valence bands InGaAs.

base/collector junction is negligible, while the conduction band discontinuity (ΔE_V) is ~.2 eV. The band alignments between $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}/GaAs$ for the devices fabricated in this work are shown in figure 4-3 and figure 4-4.

The transistor structures for this work were grown by metal-organic chemical vapor deposition (MOCVD) using an Emcore D180 system. The structures of HBTs fabricated are shown in tables 4-1, 4-2, 4-3. The structure of the DHBT fabricated is shown in table 4-4. The finished devices were large area devices fabricated using a standard triple mesa process, and tested using an HP 4145 semiconductor parameter analyzer. The samples were prepared by oxide removal with 20:1 H_2O/29.5 % NH_3OH for 30 seconds, followed by a dehydration bake at 120°C for 3 minutes. The photoresist used was AZ4330. The resist was spun at 4,000 RPM for 30 seconds, and then hotplate baked at 90°C for 90 seconds. For edge bead removal the resist was exposed for 60 seconds, and then developed in 1:5 AZ400k for 120 seconds. Pattern exposure was for 6.5 seconds (181.4 mj/cm^2). The pattern was then developed for 150 seconds in 1:5 AZ400k for 150 seconds. Samples were descummed after pattern development in an LFE PDS/PDE 301 barrel etch at 850 mtorr and 5 watts for 4 min. Prior to wet etching, the samples were postbaked at 120°C for 3 minutes (to enhance photoresist adhesion). Before wet etching and metal deposition, oxide was removed with 20:1 H_2O/29.5 % NH_3OH for 30 seconds.

The solutions used to etch the devices were 1:4:45 (50 Å /sec on GaAs) and 1:4:495 (5 Å /sec on GaAs) 85% H_3PO_4/30% H_2O_2/H_2O. The etches were used to expose the base and subcollector so that contact metal could be deposited on the emitter, base,

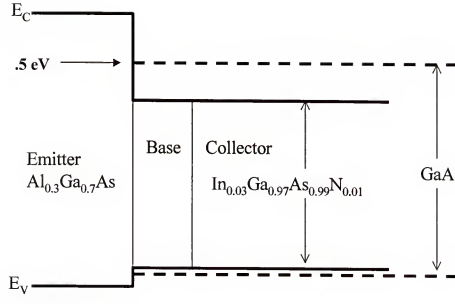


Figure 4-3: $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ heterojunction bipolar transistor.

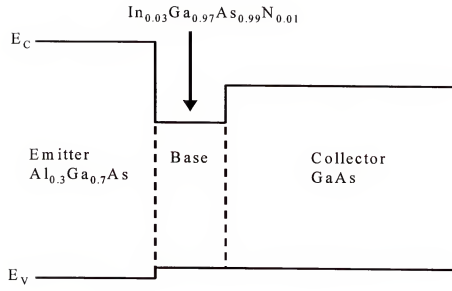


Figure 4-4: $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}/GaAs$ double heterojunction bipolar transistor.

Table 4-1: The structure of the $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ heterojunction bipolar transistor. The spacer layer is $Al_{0.3}Ga_{0.7}As$.

	Material	Thickness [nm]	Doping [cm^{-3}]
Contact Cap Layer	p^+ GaAs	200	2.00E+19
Emitter Layer	p $Al_{0.3}Ga_{0.7}As$	100	3.00E+18
Spacer Layer	u- $Al_{0.3}Ga_{0.7}As$	5	*Undoped*
Base Layer	n $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$	100	1.20E+18
Collector Layer	p^- $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$	300	2.00E+18
Subcollector Layer	p^+ GaAs	500	2.00E+18
Substrate	S. I. GaAs		

Table 4-2: The structure of the $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ heterojunction bipolar transistor. The spacer layer is GaAs.

	Material	Thickness [nm]	Doping [cm^{-3}]
Contact Cap Layer	p^+ GaAs	250	2.00E+19
Emitter Layer	p $Al_{0.3}Ga_{0.7}As$	95	3.00E+18
Spacer Layer	*u*-GaAs	5	*Undoped*
Base Layer	n $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$	100	1.20E+18
Collector Layer	p^- $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$	300	2.00E+17
Subcollector Layer	p^+ GaAs	750	2.00E+19
Substrate	S. I. GaAs		

Table 4-3: The structure of the $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ heterojunction bipolar transistor. The spacer layer is GaAs, and the base layer is graded.

	Material	Thickness [nm]	Doping [cm^{-3}]
Contact Cap Layer	p^+ GaAs	305	2.00E+19
Emitter Layer	p $Al_{0.3}Ga_{0.7}As$	123	3.00E+18
Spacer Layer	u-GaAs	5	*Undoped*
Base Layer	n $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$	92	7E+17-- >4.5E+18
Collector Layer	p^- $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$	277	2.00E+17
Subcollector Layer	p^+ GaAs	884	2.00E+19
Substrate	S. I. GaAs		

Table 4-4: The structure of the $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}/GaAs$ double heterojunction bipolar transistor. The collector is GaAs.

	Material	Thickness [nm]	Doping [cm^{-3}]
Contact Cap Layer	p^+ GaAs	200	2.0×10^{19}
Emitter Layer	p $Al_{0.3}Ga_{0.7}As$	100	3.0×10^{18}
Spacer Layer	u- $Al_{0.3}Ga_{0.7}As$	5	*Undoped*
Base Layer	n $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$	100	1.2×10^{18}
Collector Layer	p^- GaAs	500	3.0×10^{16}
Subcollector Layer	p^+ GaAs	500	2.0×10^{19}
Substrate	S. I. GaAs		

and subcollector surfaces. For the p-type ohmic contact to the emitter and collector nonalloyed Pt/Ti/Pt/Au (100 Å /200 Å /100 Å /600 Å) was deposited. For the base, Pd/Ge/Au (100 Å /500 Å /2,000 Å) was deposited and annealed at 175°C for 1 h. The HBTs were fabricated in a rectangular geometry, with an emitter area of 100x100 μm. The DHBT, however, was fabricated using a circular geometry with an emitter diameter of 50 μm. A general device cross-section is shown in figure 4-1.

Since $In_{.03}Ga_{.97}As_{.99}N_{.01}$ is new, material growth is not well characterized. Therefore, a reliable and fast method had to be used to determine HBT structure layer thicknesses, while wasting little material or needing extra investment. The easiest way we employed used the large area HBT mask to deposit ohmic contacts to the cap region. They were subsequently used to monitor etch progress. Specifically, image reversal with the emitter mesa mask level was used to deposit ohmic contacts to the cap layer. The image reversal process used AZ5214. The sample was cleaned in 20:1 H_2O/29.5% NH_3OH for 30 seconds, then dehydration baked. The photoresist was spun at 4000 RPM for 30 seconds, and then baked at 110°C for 90 seconds. Pattern exposure was for 2.45 seconds (66 mj). The wafer was then baked at 110°C for 45 seconds, and then flood exposed for 45 seconds. The pattern was developed in 1:1.4 MIF 312:H_2O for 60 seconds. This was followed by LFE photoresist descum, and 20:1 H_2O/29.5 % NH_3OH rinse. Then we used positive tone lithography (using AZ4330 photoresist) with the base mesa mask level to deposit a passivating photoresist layer over the contacts. This was done to prevent galvanic effect etching (see chapter 1). The sample was then etched for short periods in 1:4:45 and 1:4:495. Between etchings, a probe was used to dislodge the passivating photoresist from two adjacent contacts. Then, clean probes were used to

measure the current flow between them, using a Hewlett Packard 4145 semiconductor parameter analyzer. New contacts were used in each successive etching. This process is shown in figure 4-5.

Etch progress was interpreted by current vs. voltage curves between contacts after etching. When the etch proceeded within the cap/emitter layers, the current voltage characteristics were ohmic. However, as the cap/emitter layers thinned they became more resistive. This is shown in figure 4-6. When the etch reached the base layer, the resultant current voltage characteristic was that of back to back diodes (see chapter 1). When the etch reached the collector, current flow was essentially cutoff. This is shown in figure 4-7. Since the subcollector region was thick, a simple overetch was usually sufficient to uncover the subcollector. Usually, because of the difference in doping between the collector and subcollector, probes directly on the etched surface could be used to determine subcollector position. The contact of the probes directly to the subcollector semiconductor would be ohmic.

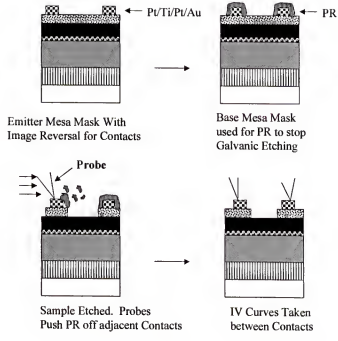


Figure 4-5: Determination of HBT structure by etching the sample, and then passing current between two Pt/Ti/Pt/Au diodes.

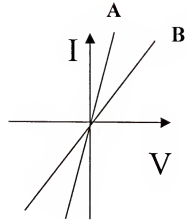


Figure 4-6: Current vs. Voltage curves for ohmic contacts to cap layer. The area between the contacts is etched within the cap/emitter region. Line B shows greater resistance than A, because more cap/emitter has been etched away.

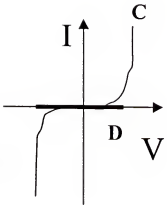


Figure 4-7: Current vs voltage curves for etch into base and collector region between ohmic contacts. When the etch reaches the base region, back to back diode characteristics are seen (Curve C). When the etch enters the collector, the current is cut off (Curve D).

4.4 Results and Discussion

The IV characteristics and gummel plots of the fabricated devices are shown from figure 4-8 to figure 4-15. In figure 4-8 and figure 4-9 the electrical characteristics for an $Al_{0.3}Ga_{0.7}As/In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ HBT with an $Al_3Ga_{.7}As$ spacer are shown (specific structure in Table II). From the gummel plot of figure 4-8 a max current gain (β) of 23 is shown. Also the V_{ON} (defined as the bias at which the collector current exceeds 1.0 μA), is .77 V. This important figure of merit demonstrates the usefulness of $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ for low power applications. The InGaAsN V_{ON} is significantly lower than the 1.03 V measured for an $Al_{0.3}Ga_{0.7}As/GaAs$ HBT of similar structure. From the IV characteristics of figure 4-9 we see that the offset voltage (V_{offset}) of the device is 280 mV, and the saturation voltage (V_{sat}) ranges from .65 to 1.20 V. These values are higher than would be expected for a device with low V_{ON} and $1.2x10^{18}$ base doping (N_{DB}). This seems to indicate that the material quality of the $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ is not as ideal as GaAs, and still needs improvement. This conclusion is supported by the $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ base sheet resistance (R_{BS}) and electron mobility (μ_n). The sheet resistance of the $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ is about 4 kΩ/sq. At 350 cm^2/Vs, the $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$ mobility is much smaller than the 2,000 cm^2/Vs mobility usually observed in GaAs. However, since the base contact resistance is scaled by the transfer length ($L_T \approx .3$ μm), the contact resistance is actually quite good at $\sim 3.9X10^{-6}$ Ω-cm^2.

Next, it was decided to fabricate variations on the same structure to see if the performance of these devices could be enhanced. The spacer layer was changed to GaAs

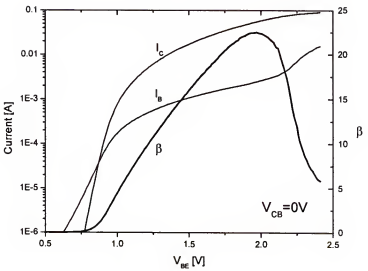


Figure 4-8: The Gummel plot of AlGaAs/InGaAsN PnP HBT. The spacer layer is $Al_{0.3}Ga_{0.7}As$. Structure corresponds to Table I. The device geometry has a 100x100 μm square emitter.

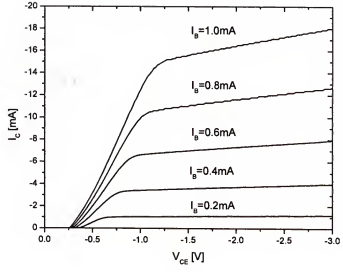


Figure 4-9: The common-emitter IV characteristics of AlGaAs/InGaAsN PnPHBT. The spacer layer is $Al_{0.3}Ga_{0.7}As$. Structure corresponds to Table I. The device geometry has a 100x100 μm square emitter.

in one structure (shown in table 4-2), and a GaAs spacer layer in combination with graded base layer doping was tried in another (structure in table 4-3). The results for these two devices are shown in figures 4-10 and 4-11 and figure 4-12 and 4-13 respectively. As would be expected, in figures 4-10 and 4-12 the V_{ON} is essentially unchanged (from figure 4-8) for the new device structures at .75 V and .76 V respectively. However, by comparing figure 4-10 to figure 4-8, it can be seen that the GaAs spacer layer actually degrades device performance. The max gain (β) drops to ~15. However, when figure 4-10 is compared to figure 4-12, the max gain (β) increases from ~15 to ~23.5. This shows that the graded base layer has a large positive effect on device performance. This is due to the built-in electric field established by the graded base doping. This field helps accelerate carriers through the base, making them less likely to be lost to recombination centers there.

In figures 4-11 and 4-13, the IV characteristics for the GaAs spacer layer devices confirm the conclusions drawn from the offset voltage (V_{offset}) of figure 4-9. For both GaAs spacer layer devices (structures in table 4-2 and table 4-3) the offset voltage (V_{offset}) of the device is 240 mV. Direct comparison of the saturation voltage (V_{sat}) ranges from figures 4-11 and 4-13 to figure 4-9 are harder, because both device geometry and emitter cross section change. However, the need to improve material quality is once again indicated by the shallow slope of the IV curve as it approaches saturation.

A final structure we tested is the $Al_{0.3}Ga_{0.7}As$ /$In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$/GaAs DHBT (structure in Table 4-4). Using GaAs as the collector material (instead of $In_{0.03}Ga_{0.97}As_{0.99}N_{0.01}$) allows a larger base/collector junction reverse breakdown voltage.

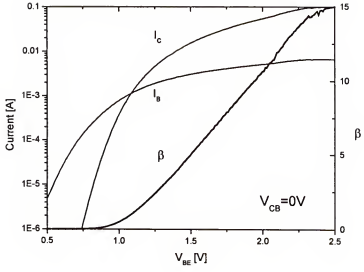


Figure 4-10: The Gummel plot of AlGaAs/InGaAsN PnP HBT. The spacer layer is GaAs. Structure corresponds to Table II. The device geometry has a 25 μm diameter circular emitter.

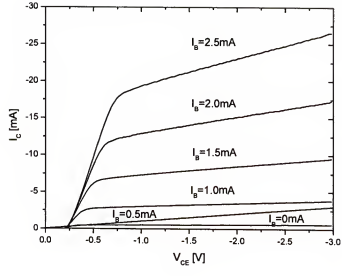


Figure 4-11: The common-emitter IV characteristics of AlGaAs/InGaAsN PnP HBT. The spacer layer is GaAs. Structure corresponds to Table II. The device geometry has a 25 μm circular emitter.

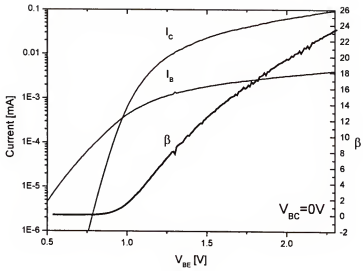


Figure 4-12: The Gummel plot of AlGaAs/InGaAsN PnP HBT. The spacer layer isGaAs, and the base layer is graded. Structure corresponds to Table III. The device geometry has a 25 μm circular emitter.

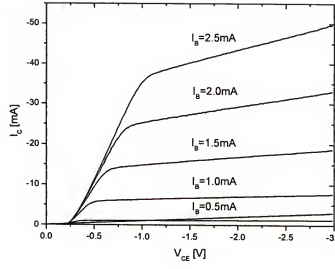


Figure 4-13: The common-emitter IV characteristics of AlGaAs/InGaAsN PnP HBT. The spacer layer is GaAs, and the base layer is graded. Structure corresponds to Table III. The device geometry has a 25 μm diameter circular emitter.

However, by looking at Figure 4-4, we can see that the unique band structure of this DHBT should have all of the advantages of both the HBT and DHBT devices, without the usual disadvantages. The large conduction band discontinuity (ΔE_C) at the emitter/base junction suppresses electron injection into the emitter thus increasing gain (β). However, there is negligible valence band discontinuity at either the emitter/base or base/collector junctions (ΔE_V). This is perfect for hole transport in p-type devices. In fact, the lack of a barrier to hole transport at the base/collector junction overcomes a problem typical to DHBT devices. Often, in DHBT devices, band discontinuities to the majority carrier at heterointerfaces decrease gain (β). However, the larger band gap of GaAs manifests itself as a conduction band discontinuity (ΔE_C) at the base collector junction, allowing the larger reverse breakdown voltage to be realized than in the HBT structure (without hurting p-type gain).

From Figure 4-14 we see that the gain ($\beta \cong 25$) of the DHBT is similar to the comparable emitter/spacer/base HBT structure of Figure 4-8 ($\beta \cong 23$). The V_{ON} of this device is .79 V, which is comparable to the $In_{.03}Ga_{.97}As_{.99}N_{.01}$ HBT structures, and much less than the 1.03 V measured for a comparable $Al_{.3}Ga_{.7}As$/GaAs HBT. However, because GaAs is used as the collector layer, the emitter/collector breakdown voltage (BV_{CEO}) is about 12 V. This breakdown voltage is comparable to an $Al_{.3}Ga_{.7}As$/GaAs HBT of similar thickness and doping level.

The $In_{.03}Ga_{.97}As_{.99}N_{.01}$ material quality issues facing DHBT are no different than in previous structures. The base sheet resistance was similar to the previously stated values, and is evidenced by the shallow slope of the common emitter IV curves as they

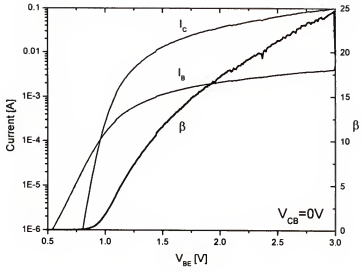


Figure 4-14: The Gummel plot of AlGaAs/InGaAsN/GaAs PnP DHBT. Structure corresponds to Table IV. The device geometry has a 50 μm diameter circular emitter.

approach saturation in Figure 4-15. The offset voltage (V_{offset}) of this device is also comparable to $In_{.03}Ga_{.97}As_{.99}N_{.01}$ HBT devices at 260 mV.

In general, all the $In_{.03}Ga_{.97}As_{.99}N_{.01}$ devices tested in this work have a gain (β) between 15 and 25. However, typical $Al_{.3}Ga_{.7}As$/GaAs P-n-P HBTs have a gain (β) greater than 100. Ideally then, $Al_{.3}Ga_{.7}As/In_{.03}Ga_{.97}As_{.99}N_{.01}$ HBT and DHBT device gain should be much larger than reported here. This is because the $Al_{.3}Ga_{.7}As/In_{.03}Ga_{.97}As_{.99}N_{.01}$ conduction band discontinuity (ΔE_C) is larger than the $Al_{.3}Ga_{.7}As$/GaAs conduction band discontinuity (ΔE_C); which P-n-P device gain should be exponentially dependent upon. Most likely this is a material issue, caused by recombination centers in the $In_{.03}Ga_{.97}As_{.99}N_{.01}$ base. This conclusion is supported by the high ideality factor, ~2 (see chapter 1), of the base/emitter junction of the tested devices. Surface recombination could also be limiting gain (β) since these devices are unpassivated. This is less likely, since the devices are so large, making the volume to surface area ratio high.

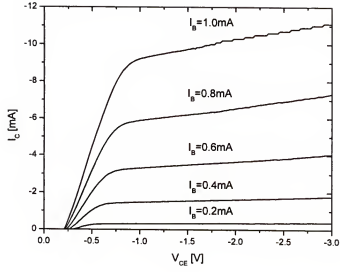


Figure 4-15: The common-emitter IV characteristics of AlGaAs/InGaAsN/GaAs PnP DHBT. Structure corresponds to Table IV. The device geometry has a 50 μm diameter circular emitter.

4.5 Conclusions

We have successfully demonstrated the first $In_{.03}Ga_{.97}As_{.99}N_{.01}$ based HBT's and DHBT. All devices tested confirmed that $In_{.03}Ga_{.97}As_{.99}N_{.01}$ can be successfully used for low power device applications. This is evidenced by substantially lower V_{ON} than a comparable $Al_{.3}Ga_{.7}As$/GaAs HBT. However, the $In_{.03}Ga_{.97}As_{.99}N_{.01}$ material needs to be improved as evidenced by the low mobility, and high sheet resistance of the tested $In_{.03}Ga_{.97}As_{.99}N_{.01}$ material. This can also be surmised from the tested devices by the higher than expected offset voltages (V_{offset}), and by the shallow slope of the IV curves as they approach saturation. Furthermore, the HBT structures demonstrated that the GaAs spacer layer (instead of $Al_{.3}Ga_{.7}As$) decreased gain, while the graded base layer greatly enhanced it. The DHBT structure demonstrated that the GaAs collector layer could be used to make the emitter/collector breakdown voltage comparable to a similar $Al_{.3}Ga_{.7}As$/GaAs HBT, without impairing the gain (β) or V_{ON} of the device. This was due to the favorable valence band (E_V) alignment of the p-type $In_{.03}Ga_{.97}As_{.99}N_{.01}$ DHBT device, which overcomes common DHBT drawbacks. From these results it can be concluded that the best device gain and voltage operating range can be obtained from a $Al_{.3}Ga_{.7}As$/ $In_{.03}Ga_{.97}As_{.99}N_{.01}$/GaAs DHBT with an $Al_{.3}Ga_{.7}As$ spacer, and graded base layer. An alternative to the graded base layer that may be just as effective may be a very thin highly doped base layer. This would reduce carrier transit time across the base, decreasing the chance for recombination, thereby increasing gain (β). Taking everything into account, the advantages of $In_{.03}Ga_{.97}As_{.99}N_{.01}$ based material in low power devices are obvious, and compatible with current foundry technology. Therefore, further research to improve the material for electronic applications is warranted.

CHAPTER 5
SPIN FIELD EFFECT TRANSISTOR PROCESSING

5.1 Introduction

The term Spintronics, short for spin electronics, refers to electronic devices where the spin direction of the electron is just as important as its charge.[28] Magnetoresistive devices that depend on electron spin are already in commercial use.[29,30] These devices are essentially material layers whose electrical resistance varies strongly with external magnetic field. They are in competition with Hall detectors and induction coils to measure magnetic fields.[30] However, spin electronic devices, which depend on spin transport, have been slow developing. That is, devices where the current has an imbalance of electron spins, and therefore a net magnetic moment during operation. The advantage of such devices is that one device could provide magnetic storage of information and electronic readout.[31] These devices may be grouped into three categories ferromagnetic semiconductor structures, magnetic tunnel junctions, and all-metal spin transistors and spin valves.[32] Ferromagnetic semiconductor structures seem the most promising of these, because of superior readout voltage in comparison to all metal devices, and fabrication requirements more favorable than magnetic tunnel junctions.[32] The spin field effect transistor proposed by Datta and Das in 1989 is such a device.[33]

The fabrication of the spin fet has proved difficult. The primary problem is that many studies have used permalloy (Ni_8Fe_2), which has been shown to be a poor spin injector (~1%).[34] Another major device consideration is spin transport length. Device fabrication will be limited by how long the electron can "remember" its spin during

transport through semiconductor material. Quantum well structures have been shown to greatly enhance spin transport length. Spin lengths greater than 100 μm have been reported.[35] Long spin transport lengths are necessary so that typical photolithography processes can be used (minimum feauture size ~1 μm). This will allow largescale commercial realization, with efficient spin injection. The availability of efficient spin injection has recently been demonstrated (using Mn as a spin aligner) based dilute magnetic semiconductors with injection efficiencies up to 90%.[36,37]

The purpose of this work is to fabricate a spin fet using conventional photolithography techniques on an InGaAs/InAlAs/InGaAs system. This will be accomplished in a two step process. First, Fe contacts will be deposited. This will quickly allow us to test different injection geometries and optimize our processing methods. It will be shown that the inclusion of an ohmic etch mask level adds great flexibility to the injection geometries that can be tested, with a single mask set. In future studies, the same mask set will be used for regrowth and testing of Mn based semiconductor spin injectors.

5.2 Background

Field effect transistors are unipolar devices meaning that they only use one type of carrier; electrons or holes to carry current through the channel. Whether the device is n or p type depends on whether the semiconductor under the contacts is n or p type. Electrons (or holes) are injected from the source contact and collected at the drain contact (figure 5-3 and 5-5). The source and drain contacts are ohmic. It is important that the contact resistance is as low as possible in order to reduce the internal power dissipation of the device, and enhance gain at lower voltages. This can be inferred from ohm's law

$$V_{ID} = I_D R$$

Here V_{ID} is the source drain voltage, I_D is the drain current, and R is the series resistance of the device. This relation holds until device reaches saturation. When the device is in saturation, further application of a Source/Drain bias will not cause a linear increase in current.

The current flow of a field effect transistor at a given V_{ID} is dictated by the gate voltage of the field effect transistor. Essentially, the schottky gate contact modulates the channel resistance of the semiconductor increasing or decreasing the series resistance. This increases or decreases the current flow in both the linear and saturation regions of the device current vs. voltage curves.

The gate controls current flow through the channel by enhancing or depleting the carrier density in the channel. Gate voltage attracts or repels electrons (or holes) from the channel. This effectively controls the channel thickness, and therefore the resistance of the channel. When the gate fully depletes the channel (there are no carriers left), no current can flow. The device is said to be pinched off. Finally, an FET reaches saturation because V_{ID} also increases the depletion region.

5.3 Experimental

The field effect transistors were fabricated using conventional lithography techniques on an InGaAs/InAlAs/InGaAS system on an InP substrate. The top layer was a highly doped 4E18 400 Å InGaAs cap layer, followed by an 3E18 300 Å InAlAs donor layer, and a 35 Å undoped InAlAs buffer layer, and a 5,000 Å undoped InGaAs channel layer on an InP substrate.

Prior to processing the sample was cleaned in 7:1 buffered oxide etch (BOE) for 1 min, and then rinsed in DI water. The sample was then dehydration baked for 3 min at 120°C. For mesa isolation shipley 1818 (2 μm) was spun at 4000 RPM for 30 seconds, and then hot plate baked at 90°C for 90 seconds. Backside clean was followed by edge bead removal. For edge bead removal the sample was exposed for 30 seconds, then developed for 30 seconds in MF 321, followed by a DI rinse. Pattern exposure was for 4 seconds (107 mj/ cm^2), and develop was for 90 seconds in MF 321. Photoresist descum was in a LFE barrell etch at 850 mTorr and 5 watts for 4 min. The sample was postbaked at 120°C for 90 seconds. Next was another BOE clean. The mesa was then etched in 1:4:45 H_3PO_4:H_2O_2:H_2O (50 Å /sec etch rate on GaAs) with 10% over etch past InAlAs. Resist removal was with acetone.

Ohmic trench etch followed next, in an effort to directly contact the 2d gas and metal. The sample was cleaned with BOE, followed by a dehydration bake. The resist, AZ 5214 (1.5 μm), was spun at 5,000 RPM for 30 seconds, and baked at 110°C for 90 seconds. Next was a back side clean and edge bead removal. For edge bead removal the sample was exposed for 45 seconds, and developed for 45 seconds in 1:5 AZ 400k:H_2O, followed by a DI rinse. Pattern exposure was for 7 seconds (190 mj/cm^2), and developed in 1:5 AZ 400k for 60 seconds. The sample was then rinsed in DI water. Photoresist descum was in a LFE barrel etch. The sample was then etched in 1:4:495 H_3PO_4:H_2O_2:H_2O (5 Å /sec etch rate on GaAs). For process method 1, the sample then had 700 Å of Fe and 200 Å of Cr deposited by MCNC (figure 5-1). For process method 2, however, the ohmic etch step and metal deposition were two separate lithography steps (figure 5-3). However, the phototlithography process for both steps is the same as the

previous, except that the ohmic etch photoresist descum was followed by a 120°C post bake for 90 seconds.

The photolithography process for the gate etch and deposition used AZ5206 (1/2 μm) photoresist. The sample was cleaned with a 20/1 H_2O/NH_4OH solution, which was followed by a dehydration bake. The photoresist was spun at 5,000 RPM for 30 seconds. It was then baked at 90°C for 90 seconds. Edge bead removal exposed the sample for 30 seconds, with a 60 second develop in 1:5 AZ400k. Pattern exposure was for 2.85 seconds (80 mj), and developed for 60 seconds in 1:5 AZ400k. Photoresist descum was again in the LFE barrel etch, followed by postbake. Since the total Donor and Buffer layer thickness is only 335 Å thick, a highly selective etch for InAlAs over InGaAs was necessary for reproducible fabrication. Such an etch (selectivity ~250) was provided by the following:[38]

1. 1gm adipic acid powder per 5ml DI
2. Add NH4OH until the pH value of the solution is 5.5
3. Add H2O2 (30%) to the pH adjusted solution at a volume ratio of about 6%

The gate metallization was Ti/Pt/Au in 200/300/1500 Å. It is important to note that for proper semiconductor etch profile (for liftoff), that the gate width be oriented along the long axis of the sample's oval defects.

The final step was bond pad deposition. The photolithography procedure was an image reversal process using AZ5214. The sample was cleaned in BOE, then dehydration baked. The photoresist was spun at 4000 RPM for 30 seconds, and then baked at 110°C for 90 seconds. Next was backside clean. Edge bead removal exposed the wafer for 45 seconds followed by 45 seconds develop in 1:1.4 MIF 312:H_2O. Pattern

exposure was for 2.45 seconds (66 mj). The wafer was then baked at 110°C for 45 seconds and then flood exposed for 45 seconds. The pattern was developed in 1:1.4 MIF 312:H_2O for 60 seconds. This was followed by LFE photoresist descum and BOE rinse. Finally, 2000 Å of Au was deposited for the pad metal.

5.4 Results and Discussion

To try to enhance spin injection into the the 2d gas of the FET we recess etched the ohmic contact pads, using the ohmic mask set (process method 1). However, even though the total etch depth was less than 1,000 Å, the lateral undercut of the mask during wet etching forbid ohmic metal contact to the 2d gas or doped cap layer or donor layer. Process method 1 is shown in figure 5-1. The gap in metal deposition was verified by SEM micrographs shown in figure 5-2 and by source drain current voltage characteristics shown in figure 5-4.

To promote ohmic contact, the next set of samples had separate levels for ohmic etch and ohmic metal deposition (process method 2). The ohmic contact level overlapped the ohmic etch level by ~2 μm. This forced the ohmic metal to contact the 2d gas donor and cap layer. This result is verified by a much larger total current flow shown in figure 5-4. The finished devices using this process method are shown in figure 5-5. The finished devices were 120 Å wide with a 1.5 μm gate. The resultant I_{ds} gate modulated curve is shown in figure 5-6. In figure 5-6 it is seen that there is ~.5 v offset voltage before the onset of current flow. This is interesting, because it is expected that most of

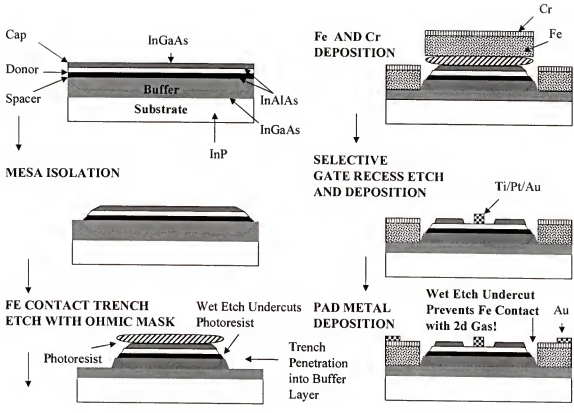


Figure 5-1: Process method 1 for Spin Fet fabrication. Use of same mask for ohmic metal etch and deposition leads to undercut of photoresist layer that prevents ohmic metal contact to 2d gas.

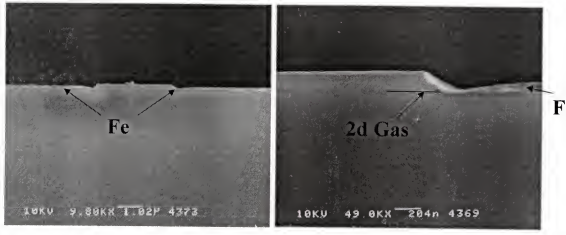


Figure 5-2: SEM micrographs of process method 1. The Fe does not contact the 2d gas.

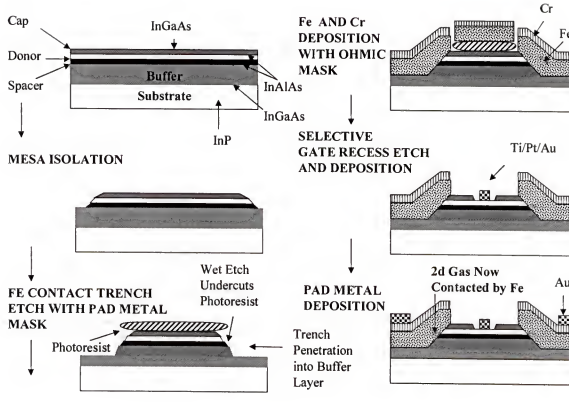


Figure 5-3: Process method 2, for spin fet fabrication. The use of separate ohmic etch and ohmic metal deposition masks allows ohmic metal to contact 2d gas layer.

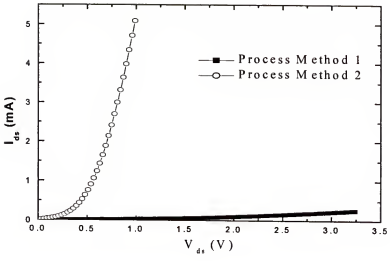


Figure 5-4: Comparison of source drain current between process method 1 and process method 2

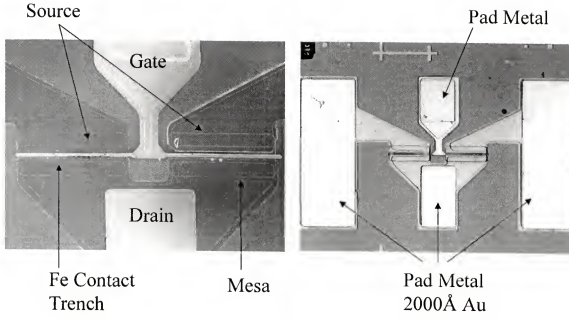


Figure 5-5: SEM micrographs of finished device.

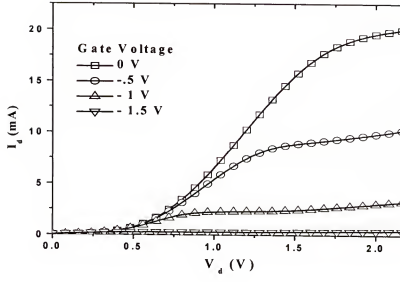


Figure 5-6: FET drain current vs. voltage curves for differing applied gate voltages. The ohmic contact metal is 700 Å Fe.

the current will be injected through the highly doped cap layer; which was ohmic to the Fe contacts. The TLM measurements made to the Fe contacted to the cap layer indicated an ohmic contact resistance of 5.2E-5 ohm-cm^2. The rectifying characteristics of the contact are due to the oxidation of the Fe ohmic contact.

It may not be desirable to inject spins through the cap layer due to spin scattering events caused by ionized impurity scattering and interfaces. By modifying the separate ohmic etch and ohmic metal deposition steps, we can now test several spin injection geometries with a single mask set that has the extra ohmic etch level. These methods are outlined in figure 5-7.

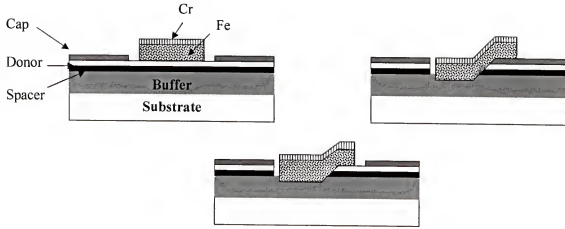


Figure 5-7: Ohmic etch profiles. Top left, no ohmic etch level, ohmic mask used for selective etch and metal deposition. Top right, ohmic etch level used to etch to buffer layer, ohmic mask metal level used to deposit metal. Bottom, ohmic metal used to selectively etch cap layer, ohmic etch level used to etch to buffer layer, ohmic metal level repatterned to deposit metal.

5.5 Conclusions

Future Fe based contacts should have a thick layer of Au (or oxygen diffusion barrier) deposited immediately after Fe deposition. Since Fe based contacts have been shown to be poor spin injectors, these process methods may be best applied to dilute magnetic semiconductor regrowth in the contact region. The same mask set can be used for both metal contact and dilute magnetic semiconductor contacts. Careful mask design allows testing of several injection geometries with the inclusion of only one extra mask level; the ohmic etch mask level. When wet etching is possible, this extra ohmic etch level allows plasma etching to be eliminated from device processing. It also eliminates undercut of the photoresist during etching that might inhibit contact formation.

The fabrication methods of this chapter, and the properties of spin injection devices, have been taken into account in designing a mask set to be used in future attempts at fabricating a spin field effect transistor by the group. This mask set not only contains the devices themselves, but also TLM strips for sheet and contact resistance, as well as a TLM like method for determining spin injection length and injection efficiency. These characteristics of the mask will be discussed in greater detail in chapter 6.

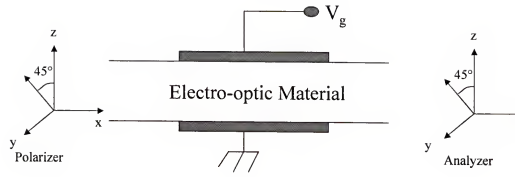
CHAPTER 6
SPIN TRANSPORT IN THE FIELD EFFECT TRANSISTOR

6.1 Introduction

The spin field effect transistor injects spin polarized current from the source that is collected at the drain of the device. The current has a net magnetic moment because there is an unbalance of electrons with up (+1/2) or down (-1/2) spin. This device essentially has two non-mixing currents (in the absence of scattering events). By using a magnetic source material to polarize the injection current, and a magnetic drain material to collect it, we arrive at the device proposed by Datta and Das. It is an electronic analog of the electro-optic modulator.[33] These two devices are depicted in figure 6-1.

In the electro-optic light modulator, light polarized at one angle is injected through the electro-optic material and is analyzed at the other end. The light output of the device depends on the relative orientation of the analyzer (which admits light polarized at only certain angles) to the orientation of the light.[33] The minimum output comes when the light is polarized 90° from the orientation of the analyzer. The orientation of the light is controlled by the gate voltage which alters the dielectric constant of the material; changing the refractive index.

The proposed spin field effect transistor performs the same function with electrons. By using a ferromagnetic contact the spins of the electron can be "polarized" by the internal magnetic field of the source contact and "analyzed" by the drain contact.



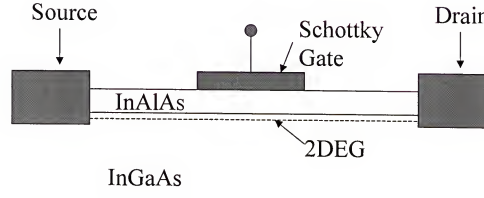


Figure 6-1: Polarizer/analyzer devices. Electric-optic modulator (Top); Spin Field Effect Transistor (Bottom). In the Spin Fet the source acts as an polarizer, the drain acts as an Analyzer. After figure by Datta.[33]

That is, the electrons will have their spins aligned to the net magnetic moment of the source contact. They will then travel through the channel and into the drain. However, at the drain, if the spins of the electrons (and source magnetic moment) are aligned anti- parallel to drain magnetic moment they will encounter an increased resistance. Therefore (neglecting channel spin flip), minimum power output occurs when the electrons have their spins rotated 180° from the orientation of the drain contact.

The spin orientation of the electrons can also be controlled by the gate in narrow bandgap semiconductor heterostructures.[33] In heterostructure FET's (like figure 6-1) the built in electric field of the interface acts on the electrons traveling in the 2DEG. Due to spin orbit coupling, this vertical electric field transforms in the plane of the 2DEG into an applied magnetic field (H*).[33] Even with no applied gate voltage this effective magnetic field is enough to cause energy splitting of the conduction band between up and down states; analogous to the Zeeman effect of bound electrons.[33] The gate can alter this electric field at the interface and therefore control the spin flip in the channel given the right conditions.

To look at gate control more closely (refering to figure 6-1), an electric field acting in the z direction acts as a magnetic field (H*) in the y direction. Electrons with their spins aligned to the y direction will gain energy, while those with spins aligned in the -y direction will lose energy. The energy of an electron conducting in the x direction in a magnetic field is:[33]

$$E = \hbar^2 k_x^2 / 2m^* +/- \eta k_x$$

Here the first term is due to the kinetic energy, while the second term is due to the effective magnetic field. Both terms are proportional to the wavenumber (k), and the effective magnetic field is proportional to the spin orbit coefficient (η).[33] This equation

implies that for two electrons (traveling in the x direction) of opposite spin to have the same energy, that their wave numbers (kx_1, kx_2) must be different. Setting their energies equal, solving for the phase difference (kx_1- kx_2), and multiplying by the mean free path (L), we obtain the phase difference ($\Delta\theta$):[33]

$$\Delta\theta = (k_{x1} - k_{x2})L = 2m^* \eta L / \hbar^2$$

For the gate to induce spin flip ($\Delta\theta=\pi$) in one mean free path, η and L must be large. Gate control enters this equation because η is directly proportional to the electric field value at the interface.[33] Also, because the phase shift dependence of any two equal energy electrons is the same, the gate should be able to achieve current modulation in multimoded devices at higher temperatures and voltages (than other quantum devices).[33] Finally, it should be noted that the phase shift equation is for one-dimensional transport only. Actual transport will have transport with components in the y direction randomizing spin. However, for potential wells with narrow widths the phase shift equation holds.[33]

The purpose of this chapter is to outline the basic physics of spin injection, and to show how spin injection may be discerned from device characteristics, and from a method similar to transmission line method (TLM) testing. These testing methods have been included in a mask design with the fabrication techniques used in chapter five. Therefore, this chapter is needed by those who continue this spin injection project for the proper fabrication and testing of future devices using the mask designed for this purpose.

6.2 Background

6.2.1 Magnetism and Conduction

To understand spin dependent transport it is first necessary to have a general understanding of magnetic materials and their properties in an applied magnetic field. The approach here will be start by explaining the basics of magnetism, and then to generalize to magnetic behavior in solids.

The magnetization (M) of a material is the net magnetic moment of a magnetic material's bound and free electrons. For bound electrons the individual magnetic moment contribution is primarily due to the magnetic field created by the electron spinning around its own axis. In free electrons an applied magnetic field causes the electrons to move in a circular path also generating a magnetic moment in addition to the spin moment. The interaction between the spin magnetic moment and the circulating magnetic moment is known as spin-orbit coupling and will be addressed in the next section. The smallest individual magnetic moment is generated by the electron spin, and is known as the Bohr magnetron (μ_B).[6]

The net magnetic moment of a material can be altered by an applied magnetic field (H). This external field is related to the net magnetic moment by:

$$M = \chi H$$

The proportionality constant χ is the susceptibility of the magnetic material. When multiplied by the external field yields M in net magnetization per volume. If χ has a negative value, then the resulting magnetization opposes the magnetic field and the material is considered diamagnetic. If the value is positive, then the net magnetization is

aligned with and reinforces the applied magnetic field and the material is considered paramagnetic.

In diamagnetic materials the induced magnetic field results from both free and bound electrons. In most crystalline solids paramagnetism is primarily resultant from electrons spinning around their own axis.[6] Spin paramagnetism usually dominates since the orbits of most electrons are locked by the lattice, and can not turn with the applied field.[6] It must be realized that materials are not purely diamagnetic or paramagnetic, but that the effects are competitive. Therefore, the total susceptibility is the sum of the paramagnetic (χ_P) and diamagnetic (χ_D) susceptibilities:

$$\aleph_T = \aleph_P + \aleph_D$$

Understanding why some materials are paramagnetic, while some are diamagnetic is important to understanding magnetic behavior in general, and spin dependent transport by extension. To do this we need to have an understanding of electron conduction at the fermi level, as well as electron density of states, and s-p orbital hybridization. The diamagnetic contribution to the susceptibility is

$$\chi_D = -e^2 Z r^2 / 6mV$$

Where Z is the to total number of electrons in the outermost subshell, r the average orbit radius, and m the electron mass. The electrons here create an opposing field to conserve energy. Only the outer electrons are counted, because the opposing field created by the outermost electrons shield the inner electrons.

It can be shown that the paramagnetic susceptibility is:

$$\chi_P = \mu_B^2 Z(E_F)/V$$

here Z is the density of states at the fermi level, and V is the volume of the material. So, it is seen that only electrons with energies close to the fermi level contribute to paramagnetism. Physically this corresponds to valence electrons. Spin paramagnetism results from the bands filling according to Hund's rule. That is, each orbital within a band must be filled with one electron with spin parallel to other band electrons, before one anti-parallel spin electron is added to each orbital (in accordance with the Pauli Principle). This maximizes the magnetic moment of the band.[6] Whether or not valence electrons have a large density of states at the fermi level results from how the electrons "fill" the band structure.

The reason why only electrons near the fermi level can contribute to the magnetic response of the material, and the extent to which a material can respond to a magnetic field is central to both magnetic response and spin polarized current. Electrons at energies below the fermi level are essentially "pinned" to that level because the states above them are already filled. However, electrons within a few ev of the fermi level can respond to an applied magnetic field. This means that electrons (near the fermi level) can switch their unfavorably aligned spins in the direction of the applied field. However, this has several consequences. First, the Pauli Exclusion principle states that only two electrons can occupy the same orbital within a band, and that they must have opposite spins. As a result, the total band structure is actually the sum of up spin and down spin band structures. Furthermore, any electron switching its spin direction must fill a higher energy level in the other band, because the states below are filled. One band has essentially lost energy, while the other has gained. However, at equilibrium, the fermi levels of the bands must be aligned, so the bands shift relative to each other (the band has

been split). Now, previously "pinned" electrons are at the fermi level and may switch to an increase in the applied field. The response to an increase in the applied field will be limited by the density (near the fermi level) of electrons left in the donating band, and the states available in the accepting band. This is shown in figure 6-2.

The two dimensional drawing of equal energy lines in the first brillouin zone helps explain the shape of the density of states vs. energy curves (figure 6-3). Here the energy increases with distance from the center. Since line lengths are proportional to the density of states, they indicate that maximum density of states is around the fermi level and decreases at low and high energies. Also, the reason for the previously stated band overlapping can be observed, in that higher band energies can be obtained along the diagonal directions.

By taking the whole discussion of paramagnetism and diamagnetism into account, we can assess the magnetic response of elements. Materials that have full, nearly full or nearly empty, valence bands (such as Au, Cu, and intrinsic semiconductors) have low density of states at the fermi level, so they are diamagnetic.[6]

A final element to spin transport is that only electrons near the fermi level can participate in conduction. To understand this, we plot the wave vectors k_y vs k_x in Figure 6-4. Here k is related to an electron's wavelength (λ) and momentum (p) by:

$$k_t = 2\pi / \lambda_t$$

$$p_t = hk_t$$

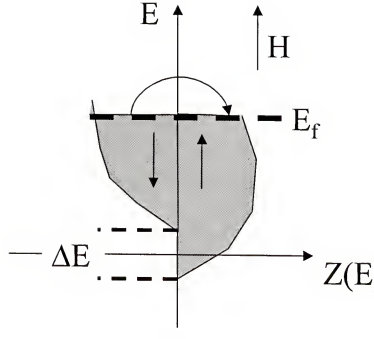


Figure 6-2: Band splitting under an applied 'up' magnetic field (H) for energy (E) vs density of states (Z(E)). Unfavorably aligned down spin electrons (left shaded region) flip spin orientations (symbolized by the curved arrow) to the 'up' alignment (right shaded region). The band splitting that occurs as a result is shown by ΔE.

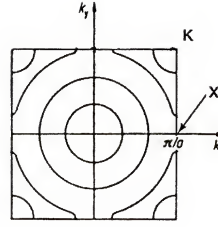


FIGURE 6-3: Two dimensional drawing of equal energy lines in the first brillouin zone explains the shape of the density of state vs. energy curve in figure 6-2. The energy increases with distance from the center.

Here, h is Plank's constant. Due to random thermal motion at equilibrium, equal numbers of electrons are diffusing in the positive and negative k_x and k_y directions, therefore the plot is symmetric around the axis (Curve A). Furthermore, the fermi energy represents the outermost point of the sphere with the interior states filled by electrons. So, all the wave vectors cancel and there is no net momentum (flow) of electrons. This is shown by the symetric shaded are of Curve A. However, when a bias is applied along the $-k_x$ direction, the effect is to shift the curve unchanged in shape along the k_x direction (Curve B).[6,8] Now, only the overlapping regions of curves A and B cancel. Therefore, there is a net change in momentum along the k_x direction near the fermi level, establishing a current flow (un-shaded area C) (figure 6-4). Now the conclusion can be drawn that since only electrons near the fermi level can change their spin orientation, and conduct, that we should be able to establish a spin-polarized current. The degree to which the injected current is polarized is proportional to the density of states at the fermi level of the up and down spin subbands of the bandsplit magnetic contact. This is done by concurrently applying magnetic and electrical fields in an appropriate material.

6.2.2 Spin-Orbit Coupling

In the previous section, it was stated that both circulating current and spin of the electron are capable of generating magnetic moments. Orbiting electrons with angular momentum act like circulating currents, and therefore generate a magnetic moment.[39] Both magnetic moments arise from the motion of the electron, so they can be addressed in terms of angular momentum. This section will explore the relationship between angular momentum, and the magnetic moment; known as spin-orbit coupling.

The angular and spin momentum of electrons is related to the principle quantum numbers of the electrons. The overall quantum number *n* designates the shell the

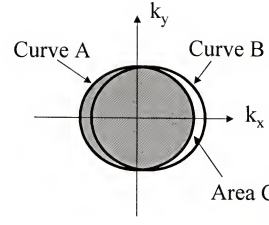


Figure 6-4: Wave vectors of electrons ky vs. kx. Curve A represents an unbiased substrate. When the substrate is unbiased there is no current flow; the curve is symetric about the axis. When the substrate is biased in the –kx direction, the curve shifts (curve B). Current now flows because the curve is unsymetric about the axis; not all vectors cancel.

electrons are located in, the quantum number l is related to the angular momentum of the electron and l can vary between 0 and n-1.[6] The individual sub-shells (bands in solids) have the following l values:

Subshell	l Value
s	0
p	1
d	2
f	3

Knowing how the sub-shells relate to angular momentum, we can calculate the total angular momentum (j) of a single electron orbital

$$j = l + s$$

The orbit angular momentum (l) and spin angular momentum (s) can either increase (s=+1/2, angular momentum are in parallel) or decrease (s=-1/2, angular momentum are antiparallel) the total angular momentum of the electron. The total angular momentum is directly proportional to, but anti-parallel with the magnetic moment.[39] This coupling of momentum and magnetic orientation is known as spin-orbit coupling. Furthermore, the high and low momentum/magnetic moment states correspond to high and low energy states. This is depicted in figure 6-5. Note that in figure 6-5 the charge of the nucleus is at right angles to the resultant momentum and magnetic field. This is important because for electrons conducting through solids, an applied field will act as a nuclear charge, and orient the resulting magnetic fields. Spin-orbit coupling allows an applied electric field in the Z direction to act as a magnetic field in the y direction (figure 6-5).

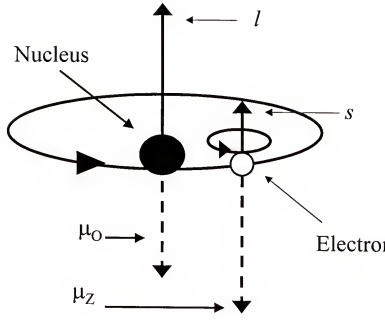


Figure 6-5: Spin-Orbit Coupling. The spin magnetic moment (μ_Z) and orbital magnetic moments (μ_O) are anti-parrallel to the spin angular momentum (s) and orbital angular momentum (l).

6.2.3 The Zeeman Effect

In the absence of a magnetic field, each up or down spin electron of momentum *l* has degenerate states equal to the number of magnetic quantum numbers *m* available to them. The permitted values for *m* are integer values between +/- *l* and 0. Therefore, the P orbital (*l*=1) has three degenerate states because *m* can be +1, -1, 0. Also, there can be two electrons paired (according to the Pauli principle) for each *m* value with spin angular (*s*) +/- ½. Therefore the P sub-shell has a maximum 6 allowed electrons.

When a magnetic field is applied to the P sub-shell, the orientation of the l angular momentum with respect to the magnetic field can take on values given by the magnetic quantum number *m*. Physically, this corresponds to three allowed non-degenerate magnetic moment vectors in response to an applied magnetic field.[39] The energies of the previously degenerate states with quantum numbers *m* are now split by the applied magnetic field. The splitting of degenerate energy levels into a number of states equal to the allowed *m* states is termed the normal Zeeman effect.[39] The normal zeeman effect is shown in figure 6-6.

As may be inferred from the previous section, the spin angular momentum also affects the total momentum and energy of the electron, causing more splitting of energy levels. This is termed the anomalous Zeeman effect. The magnetic moment associated with the spin of an electron in a magnetic field is:[39]

$$\mu_z = g_e \mu_B m$$

The g-factor (g_e=2.0023 for an electron) is the ratio of spin angular momentum to orbital angular momentum. The energy contributed by the spin angular momentum is then:

$$E = g_e \mu_B m B$$

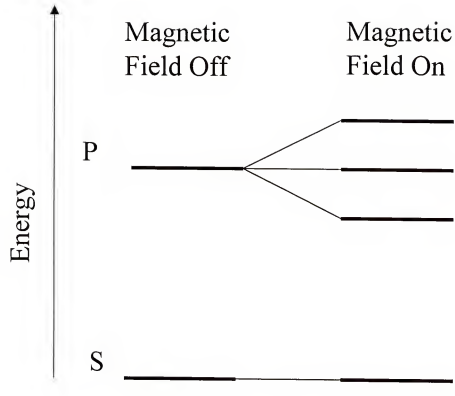


Figure 6-6: The normal Zeeman effect for the S and P orbitals. An applied magnetic field splits the degenerate levels. The S orbital is not split because it has only one allowed state.

6.3 Experimental

6.3.1 Overview

The devices will be fabricated as outlined in chapter 5 using a mask designed for this project. Different injection geometries will be tried. The spin aligners tested will be both Fe contacts, and Mn based dilute semiconductors. After fabrication the devices will be tested, at 4K, under a magnetic field to observe their resistance under different applied fields. If feasible, the spin diffusion length and injection efficiency will be resolved. The following sections give some insight into the device characteristics to be determined.

The mask designed for device fabrication and testing is shown in figure 6-7. Notice that there are TLM structures for sheet and contact resistance measurement of cap, and channel layers. There are two sets these TLM structures, one pair has ferromagnetic contacts, the other pair has non-ferromagnetic contacts. Also, there are spin orientation testers for the ferromagnetic contacts, which will be detailed in section 6.3.2 and shown schematically in figure 6-11. There are gated hall measurement test structures, and TLM-like structures for the measurement of spin diffusion length and injection efficiency. These TLM-like structures are further outlined in section 6.3.3, and are shown schematically in figure 6-13. The devices themselves are shown to be back to back fet structures (shown in figure 6-8). These devices are suitable for high speed testing. To subtract out the capacitance of the metal, "empty" devices (no active layer), are also present.

Critical mask specifications are important to know to choose correct methods for device fabrication. The TLM structures have 100X100 μm contacts, and gap spacings of 2, 4, 8, 16, and 32 μm. The TLM-like structures have gap separations of 2, 3, 4, 8, 16,

and 32 μm. The bond pads are 125x125 μm. The ohmic level etches 2 or 4 μm into the mesa. The devices have 30x100 μm. ferromagnetic drain contacts vs. 5, 10, or 20x100 μm ferromagnetic source contacts. The distance between the source and drain contacts is 5 μm. Use of the alignment marks (shown in Figure 6-9) requires understanding how the lettering beneath the alignment corresponds to the levels being aligned. The letters M, B, E, O, F, O_2, and G stand for mesa, bond pads, ohmic etch, ferromagnetic ohmic metal, final metal, ohmic metal, and gate metal respectively. Therefore, the pairing of these letters indicates that those levels are being aligned.

Figure 6-10 outlines one fabrication method for the devices based on the Fe based system outlined in chapter 5. This fabrication method may be altered for Mn based dilute semiconductor systems, but this mask set should still be applicable. For Fe based systems, mesa isolation is followed by bond pad deposition. Next, is an optional ohmic etch step, and then ferromagnetic ohmic metal deposition. The ohmic metal deposition is followed by a non-ferromagnetic ohmic metal deposition. The non-ferromagnetic ohmic metal deposition is for the Hall test structures. After, the gate level is deposited, followed by a final metal level.

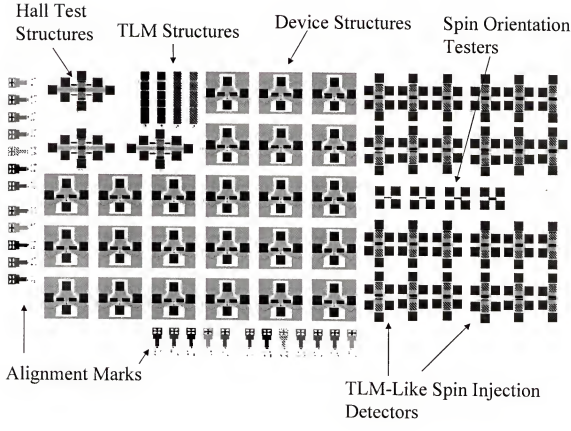


Figure 6-7: Mask designed for spin fet fabrication and testing.

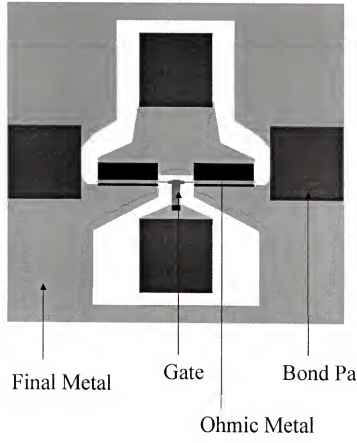


Figure 6-8: Finished spin fet. The device has two sets of 100 μm ferromagnetic contacts, with gate a length of 2 μm.

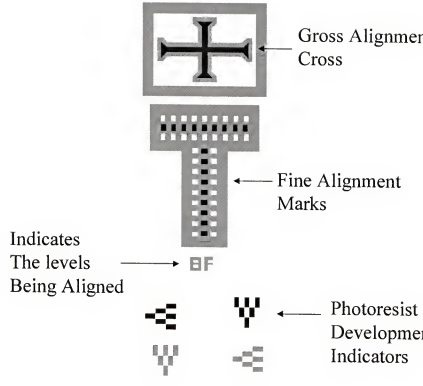


Figure 6-9: Mask alignment mark. Alignment mark resolution is .2 μm.

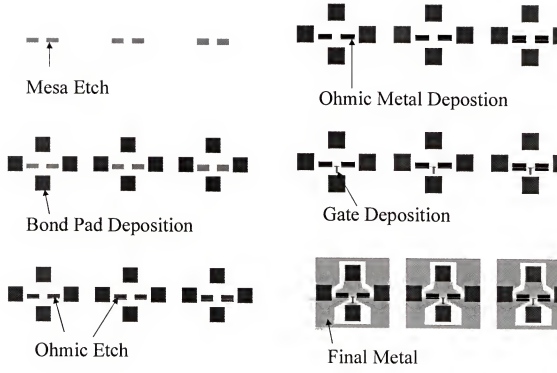


Figure 6-10: Fabrication method for the devices based on the Fe based system outlined in chapter 5.

6.3.2 Spin Transport and Resistance

By switching the spin orientations of the contacts and the channel relative to each other the resistance of the device to spin polarized flow can be altered. This is done by applying a magnetic field to source and drain contacts with different aspect ratios. Contacts with larger length to width aspect ratios switch at higher magnetic fields than contacts with small length to width aspect ratios. Generally, a thin rectangular ferromagnetic film (10-1,000 Å thick) with an aspect ratio of 4:1 or 5:1 is appropriate for single domain contact formation.[32] This anisotropy promotes an easy axis (or preferred axis) of magnetization along the long axis of the contact.[32] The field that a contact will flip its orientation at is the coercive field (H_C).

In order to verify the magnitudes of the coercive fields, the contacts need to be need to be tested individually. To do this an applied field is swept along the easy axis of the contacts in the up and down directions. While the field is swept a fixed current is passed through the length of the contact between two bondpads. Another two bond pads are used to measure the voltage drop. This is so the resistance of the wire interconnects is not included in the measurement. The minimum of resistance vs. applied field curve for the contact will signal the coercive field (H_C).[28] For sharp coercive field curves this should be tested at the minimum cryogenic temperature possible. This is shown in figure 6-11.

According to Gardelis, the low field magneto-resistance of the spin fet results from two types of effects. These "spin valve" effects result from the ferromagnetic-semiconductor interface resistance (ΔR_{CA} and ΔR_{CB} for the source/drain), and a direct resistance between the two contacts (ΔR_S) (no spin scattering).[28] Excluding the

magnetoresistance of the contacts (testing in accordance with figure 6-11 found it could be neglected), the total magnetoresistance of the device is[28]

$$\Delta R = \Delta R_{CA} + \Delta R_{CB} + \Delta R_S$$

The lowest resistance to current flow will be when both contacts and the channel are polarized in the same direction. An intermediate resistance will occur when one contact is anti-parallel to both the channel and the other contact. The highest resistance occurs when both contacts are aligned parallel and the channel is aligned anti-parallel. This is represented schematically in figure 6-12.[28]

The nature of the resistance depicted in figure 6-12 will depend on the transport regime that the spin fet is operating in. If the transport is ballistic (the electronic mean-free path is longer than the transport distance), then the spin scattering at the interfaces will dominate. This resistance modulation is termed the Giant Magneto Resistance effect

(GMR); the resistance increase for unfavorably aligned spins can be very large.[40] If transport is diffusive (the electronic mean-free path is shorter than the transport distance),

direct resistance between the two contacts (ΔR_S) dominates. In the diffusive case, spin accumulation occurs and can be dealt with thermodynamically.[41] Spin accumulation means that a spin polarized current is injected into the semiconductor faster than it can diffuse away from the interface.[41]

The overall shape of any experimental resistance vs. magnetic field curve generated will depend on the relative contributions of two spin valve effects in figure 6-12. Regardless of the transport regime, however, realizing a resistance change similar to figure 6-12 is key to realizing the spin fet in a meaningful way.

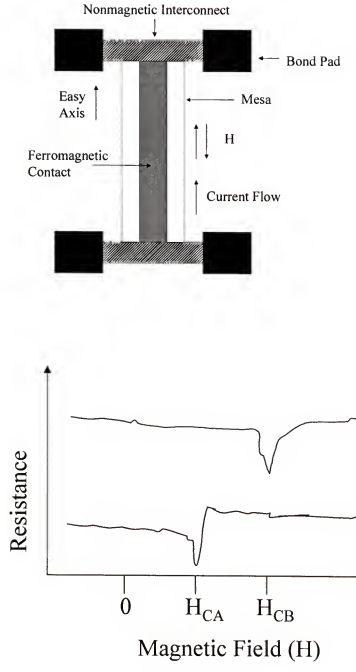
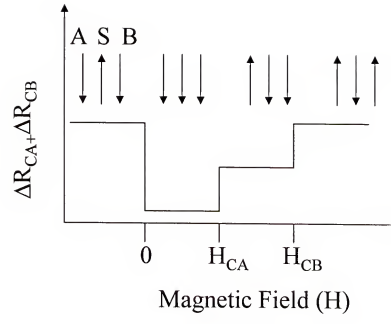


Figure 6-11: Coercive field measurements. Four terminal test structure for contact coercive field (H_C) measurements (Top). Offset curves (so they will not overlap) of expected corecive field measurements. The coercive field of the contact with the larger length to width aspect ratio is larger (H_{CB}).[28]



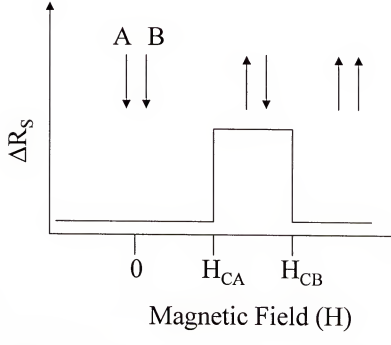


Figure 6-12: Resistance vs. Applied Magnetic Field (H) for the Spin Fet for interface (top) and direct (bottom) spin valve effects . The arrows represent the Magnetic Field Orientations of the Source Contact (A), the Semiconductor channel (S), and the Drain Contact (B). The coercive fields of the Source and Drain are denoted by CA and CB respectively. This Figure is after that of Gardelis[28].

6.3.3 Spin Flip Length

A critical limiting factor in the design of any spin polarized device is the spin flip length (δ). Spin flip length is the distance an electron can travel before it loses spin orientation. If transport is diffusive, it is related to the spin flip time constant (τ_{sf}) and diffusion constant (D) by:[42]

$$\delta = \sqrt{D\tau_{sf}}$$

where D can be obtained (for non-degenerate semiconductors) in relation to the mobility (μ), fermi velocity (v_f), and mean scattering time (τ) by:

$$D = \frac{KT}{q}\mu = \frac{v_f \tau}{3}$$

If the transport is ballistic, then the spin flip length (δ) is

$$\delta = v_f \tau_{sf}$$

For maximum effect, the spin diffusion length should be at least as long as the channel length in a FET. Therefore, for practical device applications using photolithography, a spin length of several microns is needed. In fact, spin diffusion lengths up to 100 μm have already been measured.[34]

The next section will show that to determine some physical constants in a spin device, the spin length or spin flip time constant needs to be determined experimentally, or reasonably estimated. There have been various methods used, but two resistance based measurements are by measuring the vanishing magnetoresistance as a function of distance (similar to TLM testing), and by weak antilocalization.[41,43] We will try to employ the TLM-like method.

If spin scattering at interfaces can be neglected, and if current transport is perpendicular to the surfaces, then a TLM like measurement can be used to resolve the spin flip length and spin injection efficiency.[41] This is true when the transport regime is diffusive rather than ballistic, so that interfacial scattering is a small fraction of all scattering events.[41] However, it seems Monzon and Roukes have also used this method for upper bound ballistic regime calculations.[44] The test configuration used is shown below in figure 6-13.

For distances (d) shorter than the spin flip length the equation for spin injection resistance (Z_{S1}) is[41]

$$Z_{S1} = \frac{V_s}{I_e} = \frac{\eta_1 \eta_2}{e^2} \frac{\tau_{sf} E_F}{1.5nwd} = \eta_1 \eta_2 \frac{\rho \delta^2}{wd}$$

where V_s is the voltage due to the spin injection, I_e is the total current, η_1 and η_2 are the spin injection efficiencies of the source and drain contacts, n is the density of conduction electrons, E_f is the fermi energy, d is the contact spacing, w is the width of the emitter contact. Also, the Einstein relation for the resistivity (ρ) is

$$\rho = \frac{1}{e^2 DN(E_f)}$$

where $N_{(Ef)}$ is the density of states of electrons at the fermi level. [41]

When the distances (d) are larger than the spin flip length the density of nonequilibrium spin decreases exponentially as a function of distance (d). The equation spin injection resistance (Z_{S2}) for distances longer than the spin flip length is

$$Z_{s2} = \frac{V_s}{I_e} = \left(\eta_1 \eta_2 \frac{\rho \delta}{w} \right) e^{\frac{-d}{\delta}}$$

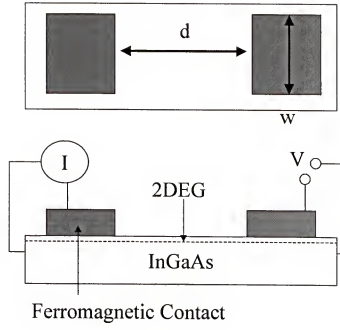


Figure 6-13: Top view of spin injection detector (Top). Side view of spin injection detector (bottom). The spin injected current is injected at one ferromagentic contact and collected at a non-ferromagnetic contact. Injected spin polarized electrons will diffuse to the other floating ferromagnetic contact registering the spin voltage (V_s).

The spin flip length can now be determined by fitting the two equations to experimental data where the distance d has been varied between the contacts. The graph of $\ln(Z_S WD)$ vs. d yields near constant $\ln(Z_S WD)$ data for distances less than the spin flip length, and a substantial drop afterward.[41]

After the experimental data is fitted to resolve the spin flip length (δ), the spin flip time constant (τ_{sf}) can be calculated from the first equations in this section. Then, we can resolve the spin injection efficiency by substituting

$$n = \frac{k_f^2}{2\pi}$$

and

$$E_f = \frac{\hbar^2 k_f^2}{2m^*}$$

into the equation for Z_{s1}. Here k_f is the fermi wave vector, and m* is the effective mass. This results in

$$Z_{S1} = \frac{\eta_1 \eta_2}{e^2} \frac{2\pi\hbar^2 \tau_{sf}}{3m^* wd}$$

For identical contacts

$$\eta_1 = \eta_2$$

As a result, by rearranging the injection efficiency can now be solved by

$$\eta_1 = n_2 = \sqrt{\frac{3m^* e^2 wdZ_{S1}}{2\pi\hbar^2 \tau_{sf}}}$$

It should be noted that this method is valid whether the contacts are aligned parallel or antiparallel, because the V ground electrode is referenced to the fermi level.[44]

6.4 Conclusions

The primary goal of this chapter was to establish the electrical characteristics of a spin fet fabricated according to the methods indicated in chapter 5 using a mask designed for this purpose. The expected resistance vs. voltage curves of a working device were established. The TLM-like method for determining spin flip length and injection efficiency, were also determined. However, its validity needs to be explored further, and other methods may need to be explored. Overall, the spin fet project for our group is just beginning, and will need considerably more investigation. Future efforts by the group seem more viable using dilute magnetic semiconductors as spin injectors. However, any progress by our group should be measured in small steps, since this device has not been realized in the 10 years since its proposal.

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BIOGRAPHICAL SKETCH

Jeffrey LaRoche was born to Frank and Lucille LaRoche on May 4, 1974, in Biddeford, Maine. After attending St. Joseph's Catholic school from kindergarten to 8th grade, he attended Biddeford High School. While at BHS he participated in track and played football. In 1992 after high school graduation he attended Worcester Polytechnic Institute in Worcester, Massachusetts, where he studied chemical engineering for four years. In order to relieve the stress of attending that school he joined Theta-Chi fraternity and also studied abroad in London, England, in the summer of 94. During this time he also met his girlfriend Caroline Kondoleon. After graduating with his B.S. in 1996 he worked for a year at Advanced Surface Technology before attending graduate school at the University of Florida in 1997. While at the University of Florida he studied semiconductors under the guidance of Dr. Fan Ren until graduation in 2000. Over the years his personality was shaped by his parents, Trevor LaRoche, Mark Moisan, Eric Vaillancourt, Nick Lombard, Michael Rupp, Dan Disalle, Michael Mastro, Caroline Kondoleon, and Keith Cloutier.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a thesis for the degree of Doctor of Philosophy.

Fan Ren, Chairman
Professor of Chemical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a thesis for the degree of Doctor of Philosophy.

Timothy J. Anderson
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This thesis was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

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